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Design and Realization of an Arc cosine Pulse Generator for Natural Switching Converter

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ABSTRACT: Static converters are used in many different areas of the conversion of electrical energy. Significant developments in electric power switches and variety of design techniques of control and regulation circuits bring very advantageous solutions for congestion, reliability, performance and maintenance of converters. The present work focuses on the study and implementation of an Arc cosine pulse generator for commutated converter acting on a composite bridge in order to linearly control the speed of a DC motor. The principle of the control of the Arc cosine pulse generator for commutated converter is based on the fact the average rectified voltage is proportional to the control voltage as the rectified voltage is a function of the average cosφ, which over a wide beach, is clearly non-linear. But for tension adjustment needs over a wide range, with a control voltage and constant ratio, it is often necessary to linearize the control. This allows a similarly linear variation in the speed of the DC motor.

KEYWORDS: Thyristor, Rectifiers ordered, Natural converter Switching, Arc cosine pulse generator.

1 INTRODUCTION

One of the key applications of power electronics is adjusting the speed of electric motors (Lander, 1988). Industrial facilities operate indeed increasingly variable speed workouts for two main reasons: to give the driven machine, the optimal speed corresponding to its various operating modes and; enslave a speaker size in equipment speed or motors acting on this equipment (Merat et *al.*, 1984; Agati, 1997). Several methods are used to achieve this objective, they vary according to the type of engine; thus in terms of induction motors, the speed variation can be achieved by the use of a dimmer, a synchronous hypo waterfall or a cyclo converter. In terms of synchronous motors, the speed variation can be achieved by the use of a self-driven synchronous machine (Dalmasso, 1988). For DC motors, the speed variation can be achieved by the use of a controlled rectifier bridge or a chopper (Lander, 1989). All these devices providing variable speed DC motors or AC allow control of the speed and limiting the current drawn. The design and realization of an arc-cosine pulse generator for commutated converter is limited to the variation of the speed of DC motors, with the aid of a controlled rectifier is to design a generator Arc cosine pulses acting on a mixed monophasic bridge with the purpose of linearly controlling the speed of a DC motor. This study is not interested in the enslavement of the problem of speed or current limitation absorbed by the motor armature. This article in its joints, first presents the material and methods title that shows in detail the control circuit of Arc cosine pulse generator and the joint bridge, then the title results and discussion and finally the conclusion.

2 MATERIALS AND METHODS

2.1 MATERIALS

For this work to be done, we used a PHILIPS oscilloscope of band width 50 MHz to visualize the different chronograms. Also a direct current motor of type C 132 SP, n° 830 776/1, of 3 kW/ 220 V and RPM 150; some thyristors and power diodes of mark SEMIKRON (SKR 71/04 and SKT 16/12C respectively) were used to ensure current flow towards the motor.

2.2 METHODS

2.2.1 POSITION OF THE PROBLEM AND STUDY OF ARC COSINE PULSE GENERATOR

For the study of the control circuits thyristor converters, three important parameters to consider. These are:

- From the gate of thyristor characteristic;
- From fashion of the converter;
- From the system control mode.

Indeed, the trigger of each thyristor must receive a control pulse well determine the frequency, amplitude, and duration in position to ensure a safe and efficient switching. While the converter operating mode allows more particularize the control circuit in the sense that it will control the converter to achieve the desired operating mode. For cons, the type of regulation is to make the system more stable and more accurate in its operation. For a priming delay φ given, the average value of the rectified voltage output from the bridge is:

-$U_{D\varphi}$= $U_{D0}\cos\varphi$: Deck while thyristor;
-$U_{D\varphi}$= $U_{D0}[1+\cos\varphi]/2$: Composite bridge;
-$U_{D\varphi}$= $U_{D0}[\cos\varphi 1+\cos\varphi 2]$: Offset Bridge.

With $U_{D0}=2V_{max}/\pi$ in single phase regime or $U_{D0}= 3V_{max}\sqrt{3}/\pi$ in three-phase system, where U_{D0} means the average rectified voltage to bridge any diode. We note that these adjusted average voltages are functions of $\cos\varphi$, which, over a wide range, is clearly non-linear. Now, for tension adjustment needs over a wide range, in a V_E control voltage, and constant ratio, it is often necessary to linearize the order, so that $U_{D\varphi}$ is proportional to V_E, that is $U_{D\varphi}= KV_E$, with K as a constant of proportionality. This allows a similarly linear variation in the speed of the DC motor.

We will show here how to linearize the characteristic of a rectifier circuit. We leave the control of a single-phase composite bridge and then generalize on a three phase composite bridge.

The average value of the rectified voltage at the output of a composite bridge is given by: $U_{D\varphi}=V_{max}(1+\cos\varphi)/\pi$. But in a reference voltage V_E, we want to $U_{D\varphi}$with constant $U_{D\varphi}=KV_E$ with constant K. For this, creating a voltage V_1 as $V_1=[V_{1M}\cos\varphi]/2 + V_{1M}/2$ that originates in the supply network as V. And assuming that $V_1=V_E$, we have: φ =Arcos $(2V_E/V_{1M} -1)K$.

Therefore, $U_{D\varphi}=V_{max} (1+ 2V_E/V_{1M} - 1) /\pi= [2V_{max}/ (\pi V_{1M})]V_E$.

By assuming that $K = 2V_{max}/ (\pi V_{1M})$, on a: $U_{D\varphi}= K V_E$.

Our work here will be to create the voltage V_1 which is an analog signal. In the following, we will associate the voltage V_E in order to make the digital signal needed to properly attack the gates of the thyristors. Therefore, we start from the block diagram in the figure below which illustrates our aspirations.

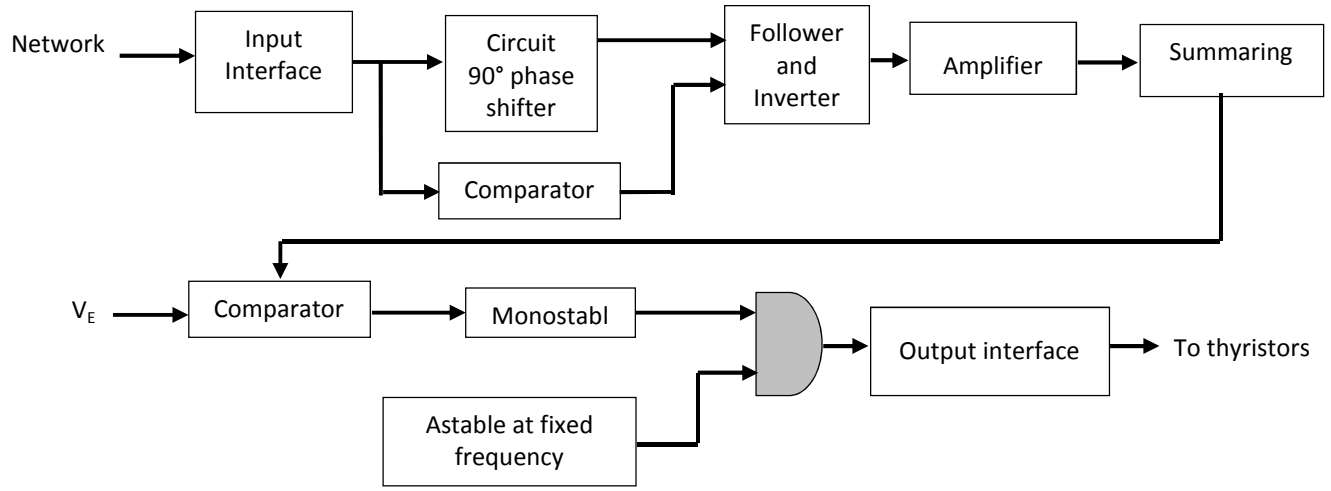

Fig. 1. General synoptic of an Arc cosine Impulse Generator.

2.3 IMPLEMENTATION OF ARC COSINE PULSE GENERATOR

From this block or the circuit of Figure 2, the interface block provides protection of the control circuit by galvanic isolation obtained by using a step-down transformer and the adaptation of the control voltage with the normalized values the voltages of the transformers. The phase shifter block of 90 ° to a transfer function $T(j\omega)=V_{A1}/V_1=[P_1^2R_3C_1^2\omega^2 - R_2]/[R_2(1+P_1^2C_1^2\omega^2)] + j[P_1C_1\omega(R_2+R_3)/ [R_2(1+P_1^2C_1^2\omega^2)]$. If $V_{A1}$is diphase from 90 ° from V_1, then $T(j\omega)$ is purely imaginary, that is to say:

$P_1^2R_3C_1^2\omega^2 = R_2$. Hence, taking $R_2=R_3$we get $P_1C_1 =\omega$. By adjusting P_1, the condition can be achieved at f= 50 Hz.

Block zero-crossing detector

The detector block of the zero crossing provides a rectangular signal depending on whether a positive or negative half cycle of V_1. If so:

- $V_1>0 \rightarrow V_{A2} = -V_{SAT} \rightarrow$ K open,
- $V_1<0 \rightarrow V_{A2} = -V_{SAT} \rightarrow$ K closed.

Inverter follower block

The inverter follower block makes it possible to its output and in function of the state of K, an inverter or a voltage V_{A1} follower. If so:

- K is open: $V_+ = V_{A1}$ and $V_- = [R_9V_{A1}+ P_2V_{A3}]/[R_9 + P_2]$.

Hence we have for $V_+= V_- \rightarrow V_{A3}= V_{A1}$.

- K is closed while $V_+ = 0$. Hence we shall have: $R_9V_{A1}+ P_2V_{A3} = 0 \rightarrow V_{A3}= - R_9V_{A1}/P_2$. By adjusting P_2 until reaching R_9, $V_{A3}= -V_{A1}$ is obtained.

Amplifier gain ½

The V_{A3} signal is bidirectional and unidirectional as we wish, it is necessary to associate a positive quantity. The V_{A3} signal is a bidirectional signal that we desire unidirectional, it is necessary to associate a positive quantity. But this addition is not without practical problems, since when V_{A3} becomes positive or zero, it is found that the operational amplifier will saturate, hence the need to first go V_{A3} in an amplifier gain half. Thus, $V_A = [R_{11}V_{A3}]/[R_{10} + R_{11}]$. Taking $R_{10} = R_{11}$, we have:

$V_A = V_{A3}/2$. We see that the ridges peak values are halved. Thus we can now superimpose a continuous magnitude for a positive unidirectional signal without saturation of the operational amplifier.

Summing non-inverting

Applying the Millman theorem V_+ and the voltage divider bridge V- in the non-inverting summing assembly, it is shown that:

$V_{A4} = [(R_{16}+R_{15})(R_{14}V_A+R_{13}E)]/[R_{15}(R_{13}+R_{14})]$.

Taking $R_{13}=R_{14}= R_{15}= R_{16}$, we have: $V_{A4} = V_A + E$. properly adjusting the value V_{1max}x E / 2, we end up $V_{A4}\geq 0$.

V_{A4}being the form of tension that research since the interval [0, π], we have: $V_{A4}(t)=[V_{1max}(1+\cos\varphi)]/2$ and V_{A4} is π, periodic, there we remains to associate a set voltage V_E, and scan the following to make it ready to attack the gates of the thyristors.

Comparator

The comparator block's role is to transform the analog signal V_{A4} obtained by a logic signal. It is annotated as the voltage V_E is the reference voltage or control that allows us to adjust the width of the comparator output V_{A5} rectangular signal. It is annotated as Zener diode D_{Z1} limits the voltage V_E to V_{Emax} value such as:

$V_{Emax} = [\pi V_{1max}U_{D\varphi max}]/[2V_{max}]$ where$V_{1max}$is the maximum voltage at the output of the adapter and the maximum voltage V_{max} of the power network. The operation of the comparator shows that:

$-V_{A4} > V_E \rightarrow V_{A5} = +V_{SAT}$

$-V_{A4} < V_E \rightarrow V_{A5} = -V_{SAT}$

Because the amplifier therefore operates in nonlinear regime, switching occurs every time

$V_{A4} = V_E$.

Monostable and astable

The fact that the output V_{A5}, the comparator generates rectangular signals and for optimization of the control signals reasons, and especially in view of the thermal dissipation of the thyristors, the astable and monostable block produce pulse signals able to effectively attack the transistor. The machine will print a suitable voltage pulse transformer which is responsible for attacking the gates of the thyristors.

Monostable

In the block shot, the $R_{24}C_3$ deriving circuit provides pulses on V- while positives pulses are shunted by diode D_7, hence triggering the shot falling edge V_{A5} with t1 of high state $t_1=[C_4(R_{25} + P_4)]\ln(V_{CC}/V_{BE})$. Adjusting the time t_1 by adjusting P_4 to adjust the duration of the pulse train that will attack the gates of the thyristors.

Astable

Against the block by the astable, the energy storage capacitor C_2 is there for the time t_2 the charging and discharging determines the operating frequency of the device, where $t_2 = R_{20}C_2\ln[1+2R_{22}/R_{21}]$. This time is used to determine the width of the control pulse of the gates of the thyristors.

From all the above, the various summary timing control circuit of Arc cosine pulse generator is as following:

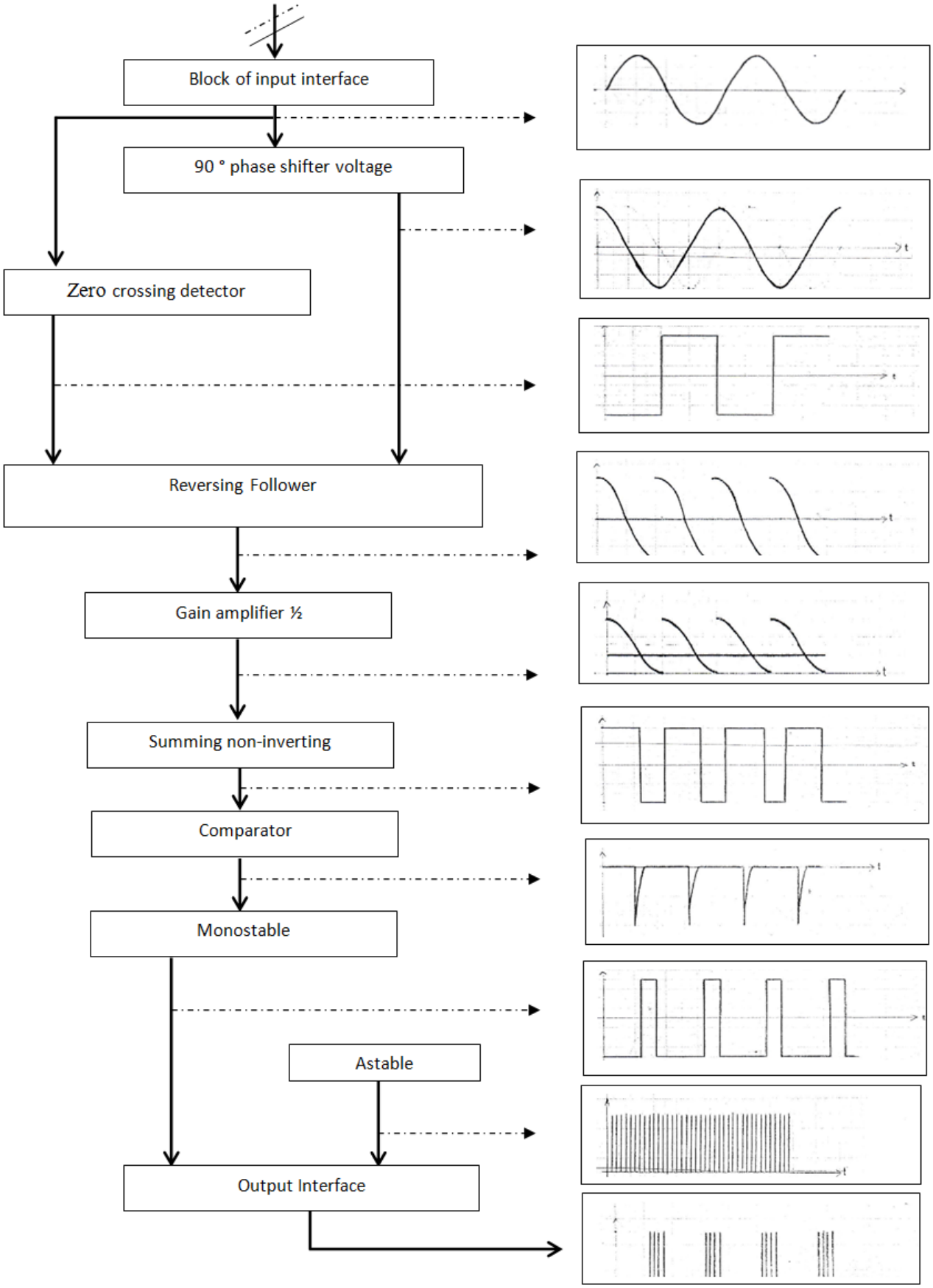

Fig. 2. Summary of the timing of the Arc-cosine Pulse Generator.

3 RESULTS AND DISCUSSION

The curves of Figures 3 to 11 show the timing of each circuit block of our converter Arc cosine pulse generator. These timing are strictly identical to those required in theory (Lander C. W., 1989). The application of this embodiment of the arc-cosine pulse generator for controlling a composite bridge rectifier previously connected to the DC motor, the characteristics of which are as follows, was more than conclusive.

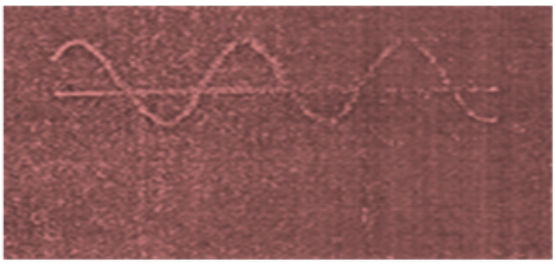

Figure 3: V_1 signal to the adapter output (5V/div.- 5ms/div.)

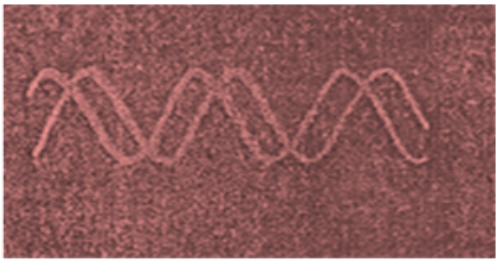

Figure 4: Signal V_{A1} superimposed V_1 to bring out the 90 ° phase shift (5V/div.- 5ms/div.)

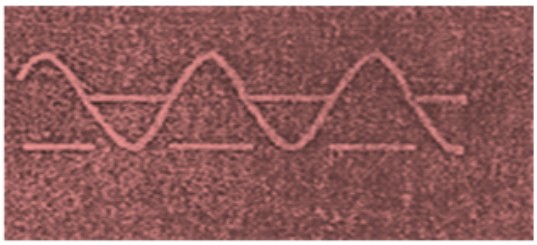

Figure 5: V_{A2} signal at the output of the zero crossing detector of V_1 (5V/div. -5ms/div.)

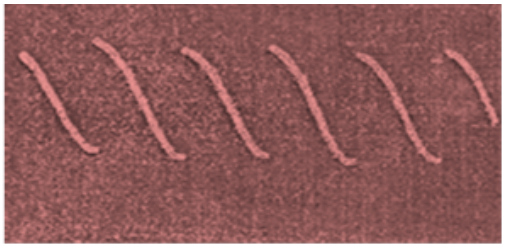

Figure 6: V_{A3} signal at the output of the inverter-follower (5V/div. - 5ms/div.)

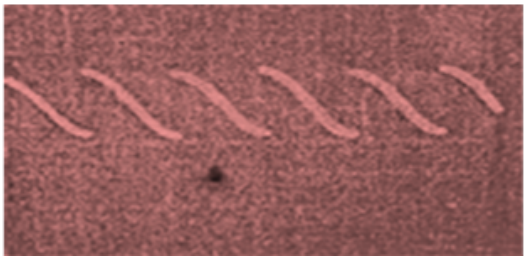

Figure 7: V_A signal at the output of the amplifier gain ½ (5V/div. - 5ms/div.)

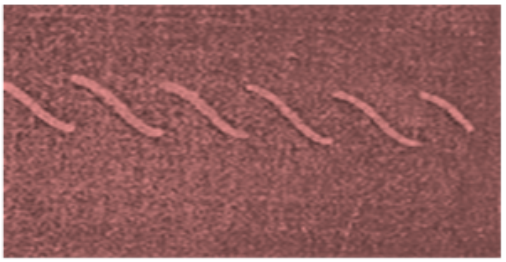

Figure 8: V_{A4} signal at the output of the summing amplifier non inverting (5V/div. -5ms/div.)

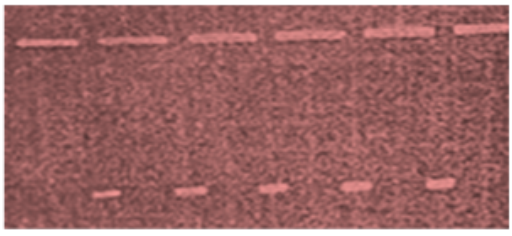

Figure 9: V_{A5} signal at the output of comparator (5V/div.- 5ms/div.)

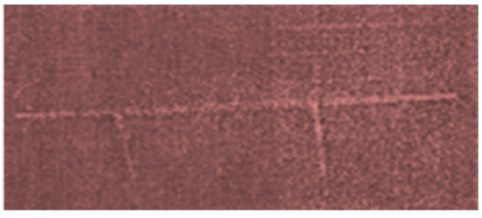

Figure 10: Pulse signal to the stable mono input to output $R_{24}C_3$ (5V/div.- 5ms/div.)

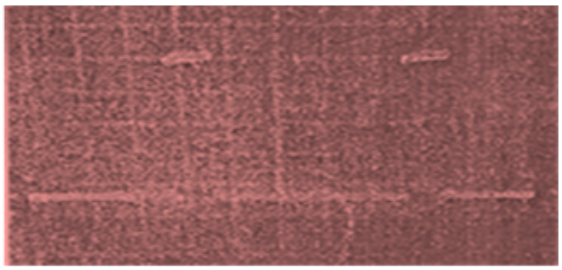

Figure 11: V_{A6} signal at the output of the monostable (5V/div. - 5ms/div.)

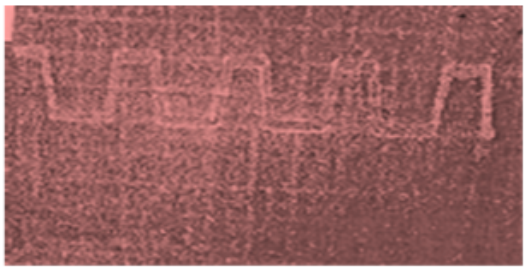

Figure 12: Signal V_{A7} à la sortie de la diode D_6 down stream of the astable (5V/div. - 5ms/div.)

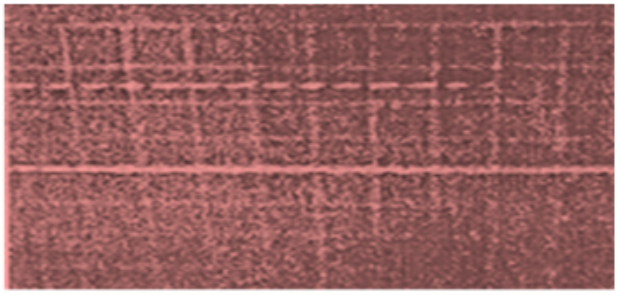

Figure 13: Train of pulses at the output of the AND gate ready to attack the base of the transistor T_{R2} (5V/div.- 5ms/div.)

Even our device worked, it was not without difficulties. When carefully observes the 12 and 13, we find that these two timing diagrams are not strictly rectangular. Figure 12 is rounded and Figure 13 is trapezoidal. All attempts to correct them have been unsuccessful. This inability is in my opinion one that is specific to the performance of certain features from discrete components. Another difficulty and not the lower was combat distortion phenomena due to the saturation of the operational amplifiers. This led us to replace the resistor R_1 by an adjustable resistor. This change allowed us to adjust the value of R_1 at a level that avoids distortions us about the different outputs of operational amplifiers. This adjustable R_1 has contributed to significantly reduce the amplitude of our signals in the control circuit, thereby reducing the range of variation of the engine speed. This difficulty can be overcome by replacing the operational amplifiers MC 1458 P which saturates at 18 V by operational amplifiers having higher saturation voltages. While our goals are met, it is necessary to perfect in terms of the supply voltage or servo motor speed to a desired size, taking into account the limitation of the current drawn by the motor armature. It is imperative to think enslave the system to be sure that our system does not include disturbances that are usually born out of the system and affect the outputs thereof, there by changing the report loses $U_{D\varphi}/V_E$ its constancy.

4 CONCLUSION

This study of the study and the realization of an Arc cosine pulse generator was designed to generate control pulses trigger a converter can be used to control the linear speed of a DC motor continuously. The results obtained are practically quite satisfactory, since all the theoretical curves that we have planned for the study was obtained virtually and in combining a DC motor with our device, we observe that from the potentiometer of the reference voltage V_E, it varies linearly engine speed. While our goals are achieved, this study is to perfect the plans of the servo power supply or motor speed considering the limitation of the current drawn by the armature. On another level, we can consider the change in speed of other types of engines other than DC motor that the DC motor is suitable for some applications but is very limited when getting stronger or well when we must work in a not very clean environment.

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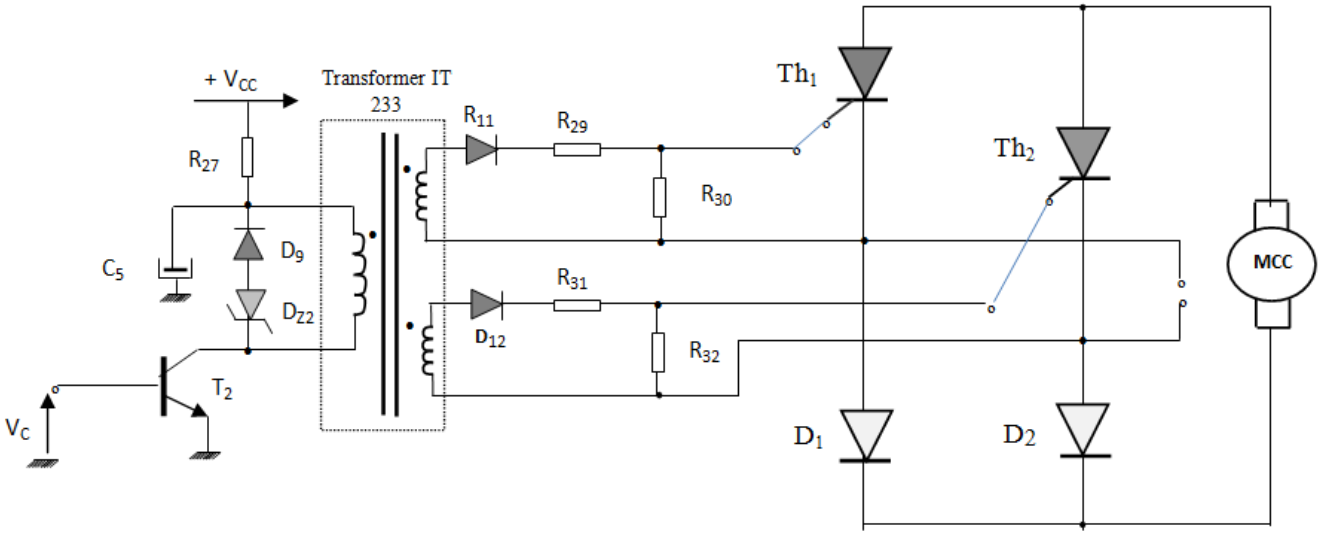
ANNEXE I. POWER CIRCUIT OF ARC COSINE PULSE GENERATOR FOR COMMUTATED CONVERTER



ANNEXE I. CONTROL CIRCUIT ARC COSINE PULSE GENERATOR FOR COMMUTATED CONVERTER (CONTINUED)