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Design of an efficient NOR Content Addressable Memory Bit cell Using memristor and MT-CMOS in FinFET Technology

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ABSTRACT: Content addressable memories (CAMs) are type of computer memory that is used in search intensive applications. It involves content based searching. The conventional CAM is designed using MOSFET, due to which the power consumption is very high because of parallel architecture and short channel Effects such as leakage current. However, the current trend is to use a new non planar device architecture, the so called FinFET to overcome the problems of planar MOSFET stated above. Among the alternatives to planar MOSFET, FinFET is proved to be more efficient in terms of power. Although the CAM using FinFET is efficient ,it is volatile. In order to make it non-volatile, a new element called memristor can be used. Also, when the device is idle,the leakage will be high. This can be overcome by the use of MT-CMOS for power gating. This paper proposes a novel design of NOR content addressable memory bit cell using memristor and MT-CMOS in 22-nm FinFET Technology. The design has been simulated in 22nm FinFET technology using Tanner EDA tool.

KEYWORDS: Content addressable memories (CAMs), FinFET, memristor, MT-CMOS, Short channel Effects, Tanner EDA, Power Gating Technique.

1 INTRODUCTION

Content addressable memories (CAMs) are computer memories, also known as associative memory that search data based on content instead of explicit address. The data to be searched is given as input to the CAM, and then the CAM compares the input data with data previously stored in the lookup table. If the data is matched, it outputs the location of the matched data within a single clock cycle. Thus it is mainly used in applications that require high speed search operations such as in translation look-aside buffers (TLBs), network routers database accelerators, image processing, parametric curve extraction, Hough transformation, Lempel–Ziv compression, image coding, virus detection and Huffman coding/decoding [3], [4]. Because of this fast searching operation in CAMs, there will be high dynamic power consumption [5] [6].This was a major problem in the CAM designed in the past. But, due to advancements in CMOS technology, leakage in memories became a huge concern [7] [8]. As the transistors are scaled in nanoscale, transistors are kept very close to each other, which increases the parasitic effects between individual circuit node than the transient behavior of memory bitcells, such as SRAMs [9][10]. When transistors are scaled to nanoscale, the conventional MOSFET started losing its property due to short channel effects. Multi-gate devices started replacing conventional MOSFETs. Double Gate FETs (DGFETs) are better substitute to planar MOSFETs as the two gates aid a better electrostatic control over the channel. FinFET is a type of DGFET that has better scalability and compatibility with the planar CMOS process [12], [13].

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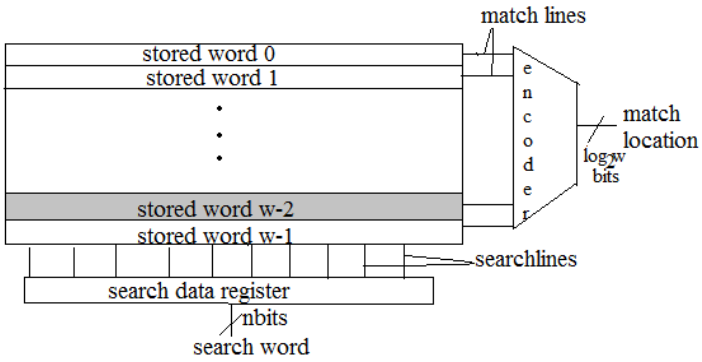


Fig 1.BLOCK DIAGRAM OF CAM

FinFETs are of three types, namely, Shorted Gate(SG), Asymmetric gate-workfunction Shorted –Gate(ASG), Independent Gate (IG). In the SG type FinFET, the two gates are shorted together and it yield largest ON current (I_{ON}).The ASG type FinFET is similar to shorted gate, but the two gates have different workfunctions. It has the same layout area as that of SG FinFET, and has lower leakage current achieved at the cost of 26% degradation in the drive current (I_{ON}). In IG FinFETs, the two gates are made independent by etching away the gate material above the vertical channel. Though the leakage current in IG FinFETs is one to two orders of magnitude lower than that of SG FinFETs (with appropriate back-gate bias), it is at the expense of a severe degradation in ION and increase in layout area due to the need to insert back-gate contacts [14]-[16].Out of the three FinFETs, SG FinFET is fast but leaky and ASG FinFET is slower but less leaky. IG FinFETs are less leaky but there is an increase in area. However, we employ SG FinFET than the other two types in designing CAM as it is superior in terms of delay and area[2].

2 CAM REVIEW

In this section, operation of the CAM and an example of its use in routing is described.

A. OPERATION OF CAM

Fig. 1 shows a simplified block diagram of a CAM. It consists of search data registers, encoder, match lines, lookup table. The input data is given to the search lines which are connected to the lookup table. All the matched lines are pre-charged to High level. The CAM bitcell compares the input bit with the stored bit. Matchlines with all bits matched maintain in the pre-charged high state. Matchlines in which at least one bit mismatch, discharges to ground. The match lines are given to an encoder that generates the match location corresponding to the matchline that is in the high state. A simple encoder is used if only one match is probable. Some CAM applications will produce more than one word as match. In such cases, a priority encoder is used instead of simple encoder [1].

B. EXAMPLE

An example of operation of CAM in Network routers is shown in Fig.2.The router has a routing table like TABLE I that has four entries. The “X” in the table denotes the “don’t care” which means X may be 0 or 1. For example, if router obtains a packet with destination address 10010, the packet is forwarded to port A. Suppose if packet with destination address 1101X is given to router, then both entry 3 and 4 matches in the lookup table. But, entry 3 is selected, since it has less X bits. The entry 3 is encoded to match location 10.This match location 10 is given as input address to RAM.RAM which contains a list of ports, outputs port 3 corresponding to input address 10. Then the packet is forwarded to port 3 [1].

TABLE I. EXAMPLE ROUTING TABLE

Entry No	Address(binary)	Output Port
1	100XX	A
2	1010X	B
3	1101X	C
4	110XX	D

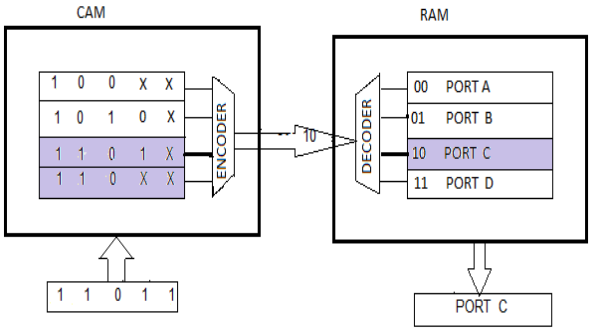


Fig2. CAM BASED IMPLEMENTATION OF ROUTING TABLE I

3 NEED FOR MEMRISTOR AND MTCMOS

While designing analog circuits, passive elements like capacitors, inductors and resistors are mostly used. But, there exists an another fundamental element called memristor which is made of semiconductor .Its resistance is called as memristance and it varies as a function of flux and current. It has many advantages: requires less energy and produces less heat. It won't consume power during idle state and are suitable with CMOS interfaces. Now, the undergoing research is how to use memristor in various analog, digital circuits, computers and sensors. For circuit level simulation, spice model of memristor is used which is efficient in terms of both size and power dissipation. In order to make CAM as non-volatile, spice model of memristor can be used. Fig.3 shows the symbol of memristor.

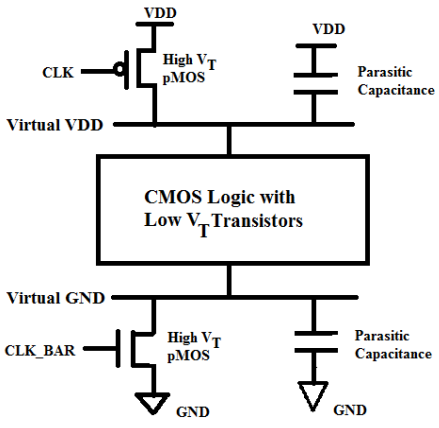


Fig.3 Symbol of memristor *Fig.3.2 Generic structure of a MT-CMOS logic gate*

Circuits based on single threshold voltage suffer from increased delay, power consumption and less responsive in producing output. These defects can be overcome by the emergence of a technique that use MOSFET with multi-threshold voltage. Most of the low power designs came into existence only with the use of this MT-CMOS Technique. The purpose of this MT-CMOS is to enable high speed operation during active mode and less power consumption during idle mode. This is achieved using both high and low threshold voltage (Vt) transistors. Low Vt transistors in the signal path as shown in Fig.3.2. reduces power dissipation without degrading the performance. High Vt transistors shown in Fig.3.2., also known as sleep

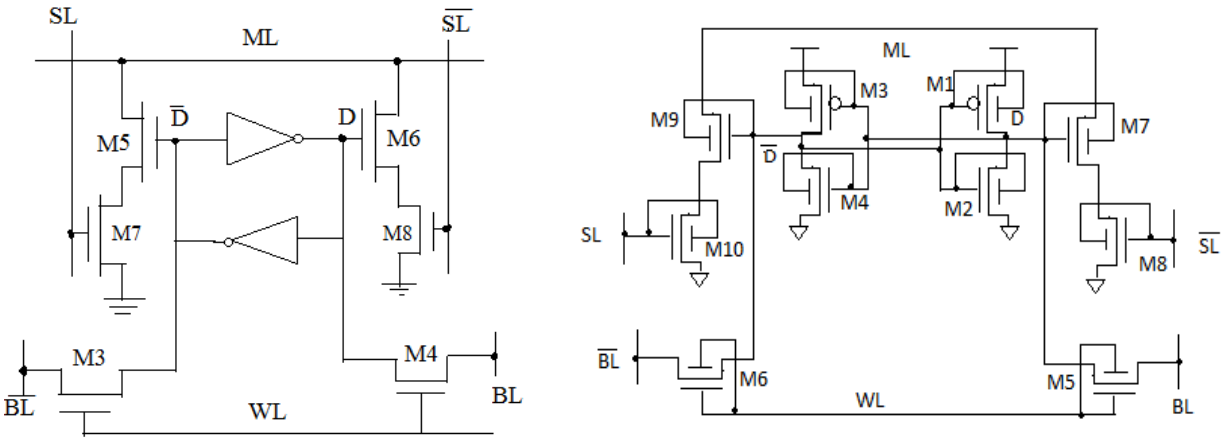
transistors, are used to isolate the circuit from the power rails so that the static power dissipation in the idle mode is reduced.

4 DESIGN OF FINFET CAM

In the architecture of CAM,the major part is CAM bitcells.In this paper,such a CAM bitcell is designed using Shorted Gate type FinFETs and memristor and MT-CMOS are included to improve its performance.

A. CAM CELL CIRCUITS

Each CAM bitcell contains two parts: a storage unit and a comparison circuitry. The storage unit is the one in which data is stored. The comparison circuit is to compare whether the search data is matched with stored data.Two types of CAM cells are used in most of the CAMs:Binary CAM cell



(a) Using conventional MOSFET *(b) Using SG FinFET*

Fig.4.1. Schematic diagram of NOR CAM bit cell

(BCAM) and Ternary CAM cell (TCAM). The BCAM cell is made of 6-9 transistors, while TCAM cell requires 12-17 transistors in standard CMOS design. Since the die area of TCAM is larger than the BCAM, BCAM is mostly preferred [1].

B. CAM USING SG FINFETS

In this paper, BCAM NOR cell is designed using ten transistors. The storage unit is made of a typical 6T SRAM cell. The comparison unit is made of XOR/XNOR matching circuitry for data comparision. CAM can be classified into NOR, NAND categories. The NOR CAM bitcell using conventional MOSFET is shown in Fig. 4.1(a), has cross coupled inverters and transistors M3 and M4 that forms the storage unit, while M5-M8transistors form the comparison unit. In the proposed diagram as shown in Fig. 4.1(b), the same NOR BCAM bitcell is designed using SG type FinFET. In that Fig. 4.1(b), M1–M6 forms the core SRAM cell, while transistors M7–M10 form the matching circuit. In the proposed architecture shown in Fig.4.2, a memristor is used in between VDD and the drain of M1 and M3. When VDD is ON, the memristor will be in cut off region. So, it transfers the charge fast down, and the CAM bit cell performs normal read and write operation. When VDD is OFF, it goes to saturation region and hence retains the data in the CAM Cell. It does not allow the normal operation such as read and write but allows to retain the data in the form of charge. The memristor is designed in 3nm technology because of less number of transistors and reduced size compared to 22nm technology. The memristor consists of comparator, multiplier and current conveyor. Here, double tail comparator is used. Thus, the proposed CAM will be equipped with non-volatile property and also it will have reduced.

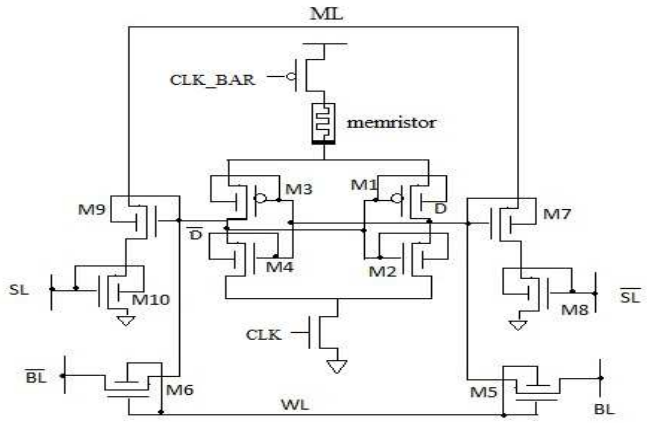


Fig.4.2 Proposed CAM bit cell using memristor

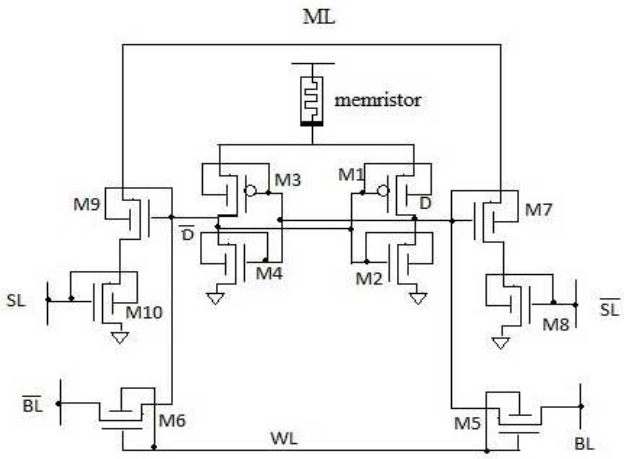


Fig.4.3 Proposed CAM using memristor and MTCMOS

Power consumption. Even though the CAM using memristor is efficient than the previous designs, the leakage still exists. When the device is idle, the leakage power increases. So, there is a need to turn off the device when it is idle. In order to achieve Even though the CAM using memristor is efficient than the previous designs, the leakage still exists. When the device is idle, the leakage power increases. So, there is a need to turn off the device when it is idle. In order to achieve this, it must be isolated from power rails.

For this, a novel architecture is proposed as shown in Fig.4.3, an additional PMOS is connected in between VDD and memristor and NMOS in between sources M2,M4 and GND. Thus, it will turn ON transistors only when CLK is enabled i.e. only when the CLK is HIGH or CLK_BAR is LOW. When the CLK is given HIGH, the device is connected to the power rails and it performs the normal operation. When the CLK is given LOW, the device is isolated from the power rails, thus reducing the leakage power. Thus, by using both memristor and MTCMOS an efficient CAM can be designed. By designing so, the average power consumption is reduced.

5 EXPERIMENTAL RESULTS AND COMPARISON

STEPS INVOLVED IN OBTAINING OUTPUT

STEP 1: CIRCUIT DESIGN USING S-EDIT

S-Edit is used to draw the schematic of the CAM bit cell. The CAM design shown in Fig.4.1(a),4.1(b),4.2,4.3 is drawn in S-Edit (Schematic Editor) of Tanner EDA as shown in Fig.5.1,Fig.5.2 and Fig 5.3 respectively. In order to draw, Predictive Technology Model (PTM) in 22nm library is used Since we use 22nm technology, the VDD required for the CAM bit cell is given as 200mv.The output is to be taken from D and D'. Then, the circuit is simulated. For Fig.4.2 and 4.3, 3nm memristor and 22nm MT-CMOS is used and the circuit is simulated.

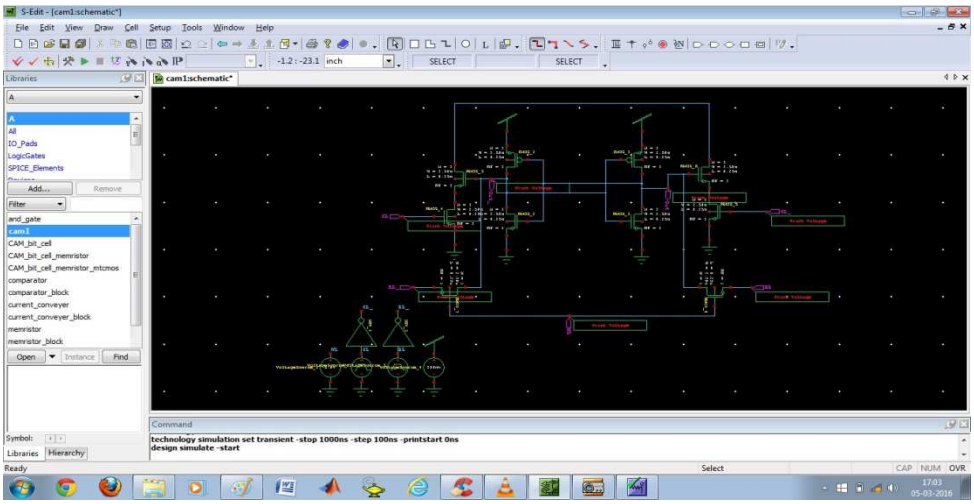


Fig.5.1 Schematic of NOR CAM bit cell using MOSFET in S-Edit Tool

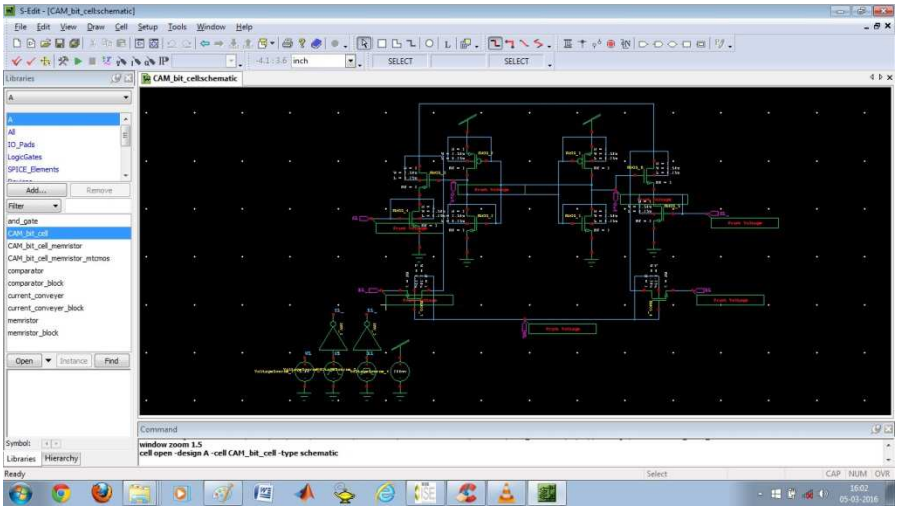


Fig.5.2 Schematic of NOR CAM bit cell using MOSFET in S-Edit Tool

STEP2: VIEWING THE WAVEFORM IN W-EDIT

After simulating the circuit in S-Edit, the W-Edit window opens and gives all the waveforms of the input and outputs such as waveforms of select line (SL,$\bar{L}$), match line (ML,$M\bar{L}$)and bit lines (BL,$B\bar{L}$) and output at D and D'(OUT,OUT_) are shown in Fig.5.5 , Fig.5.6,5.7,5.8 respectively.

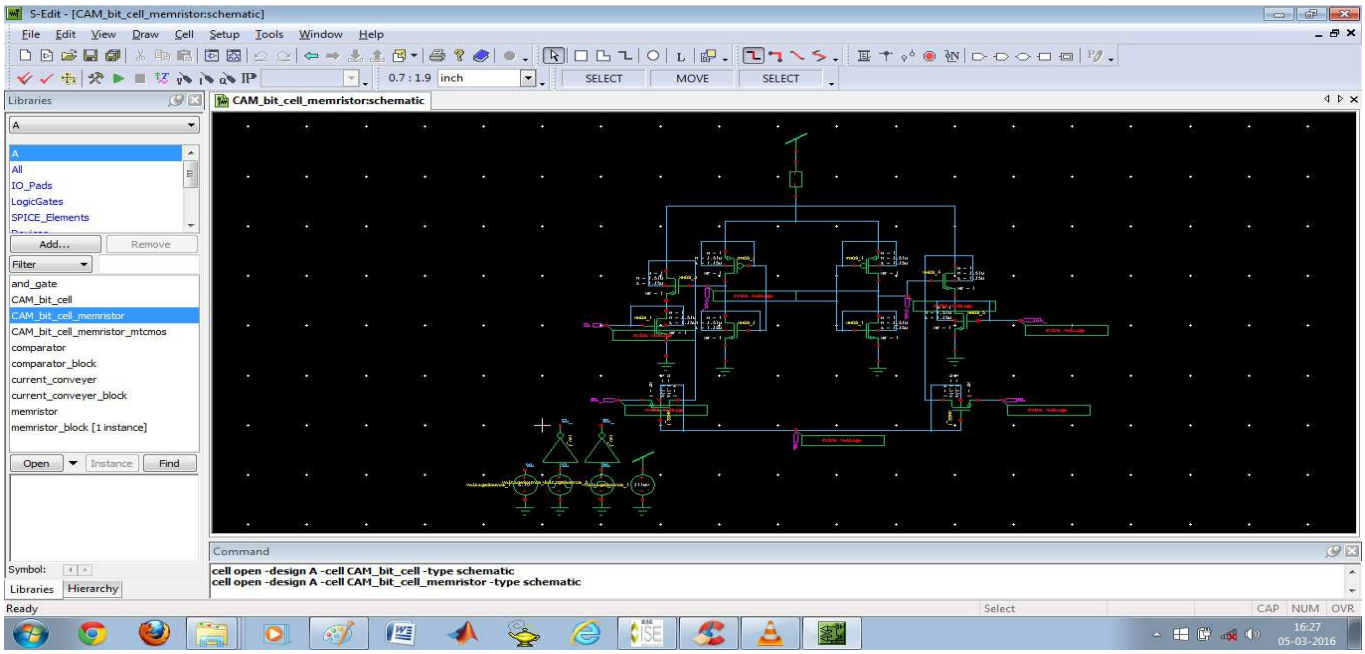


Fig.5.3 Schematic of proposed NOR CAM bit cell using memristor in FinFET Technology in S-Edit Tool

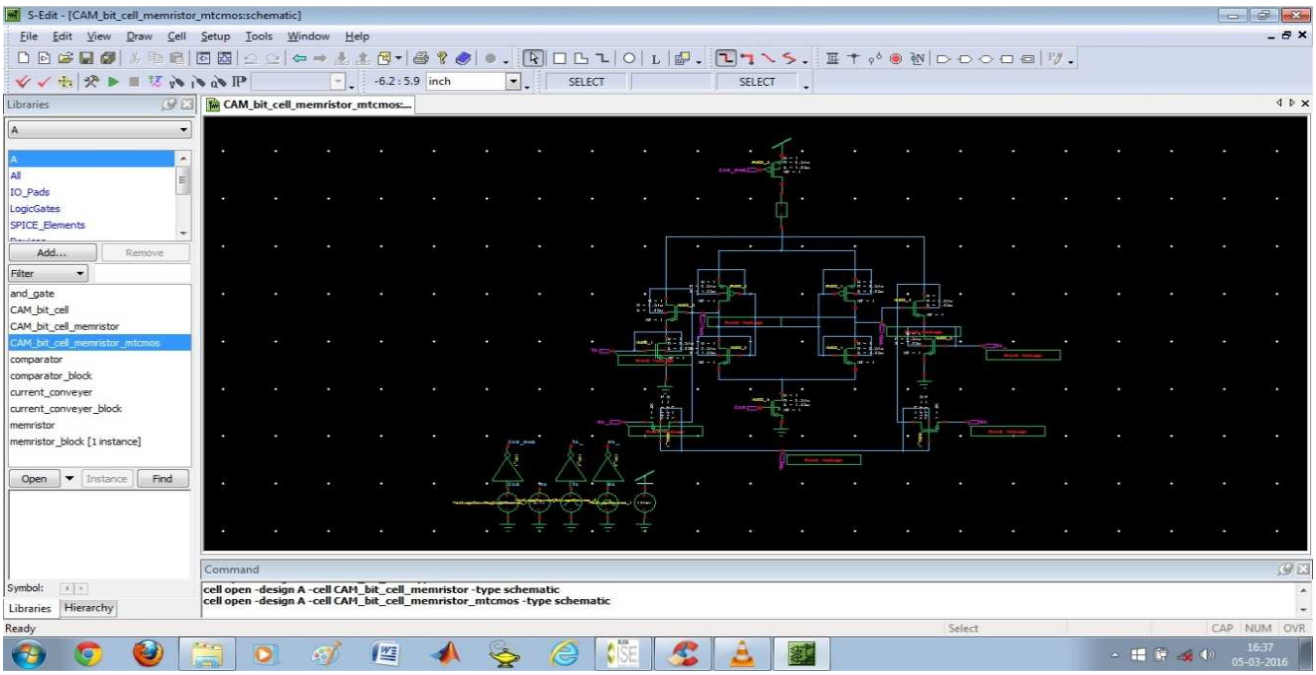


Fig.5.4 Schematic of proposed NOR CAM bit cell using memristor and MT-CMOS in FinFET Technology in S-Edit Tool

STEP 3: REPORT FROM T-SPICE

After the circuit is simulated in S-Edit Tool, it generates a code or program in T-Spice. Then, in order to find the power consumed, a code (.power) is used and temperature command (.temp) is used to obtain power in three different temperatures at 20,40 and 60 degree Celsius. Now, the T-spice code is simulated and the power outputs obtained are used for comparison as shown in TABLE 6.1. A graph is plotted for TABLE II as shown in Fig.5.9

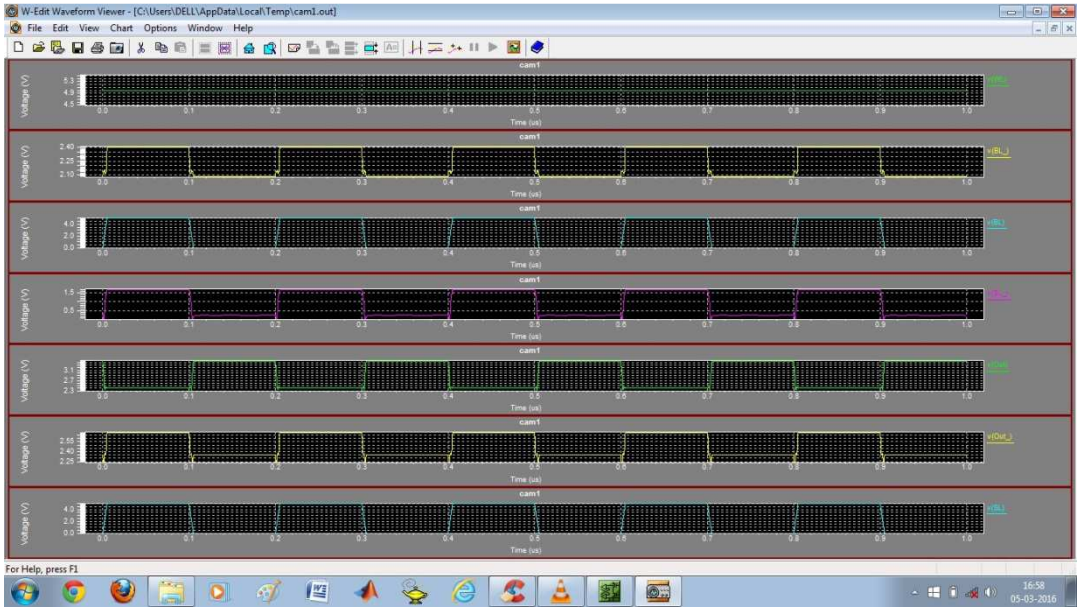


Fig.5.5 Output Waveforms of the NOR CAM bit cell using MOSFET in the W-Edit

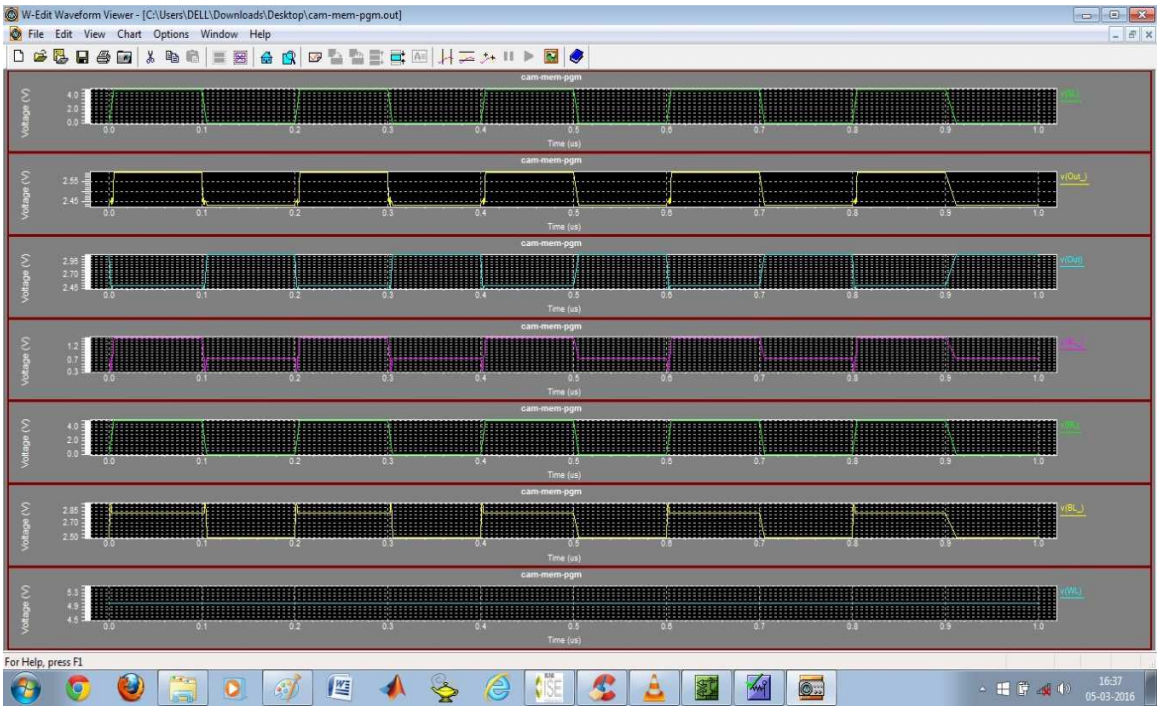


Fig.5.6 Output Waveforms of the NOR CAM bit cell using FinFET in the W-Edit

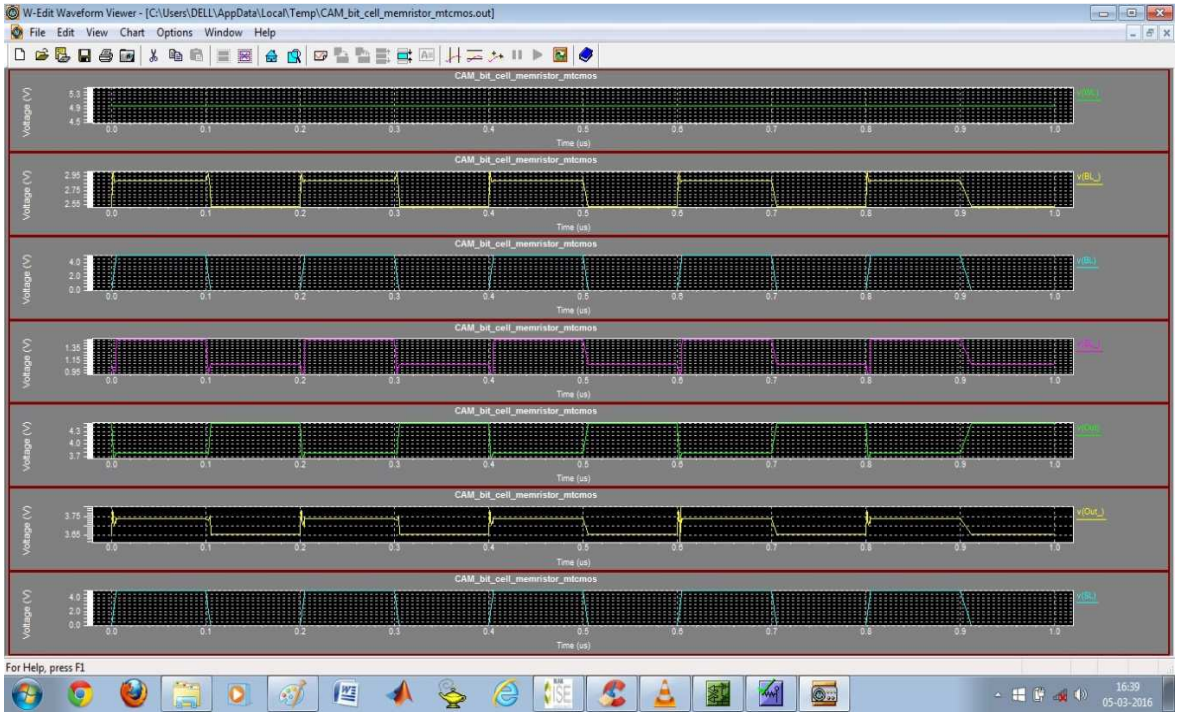


Fig.5.7 Output Waveforms of the NOR CAM bit cell using memristor in the W-Edit

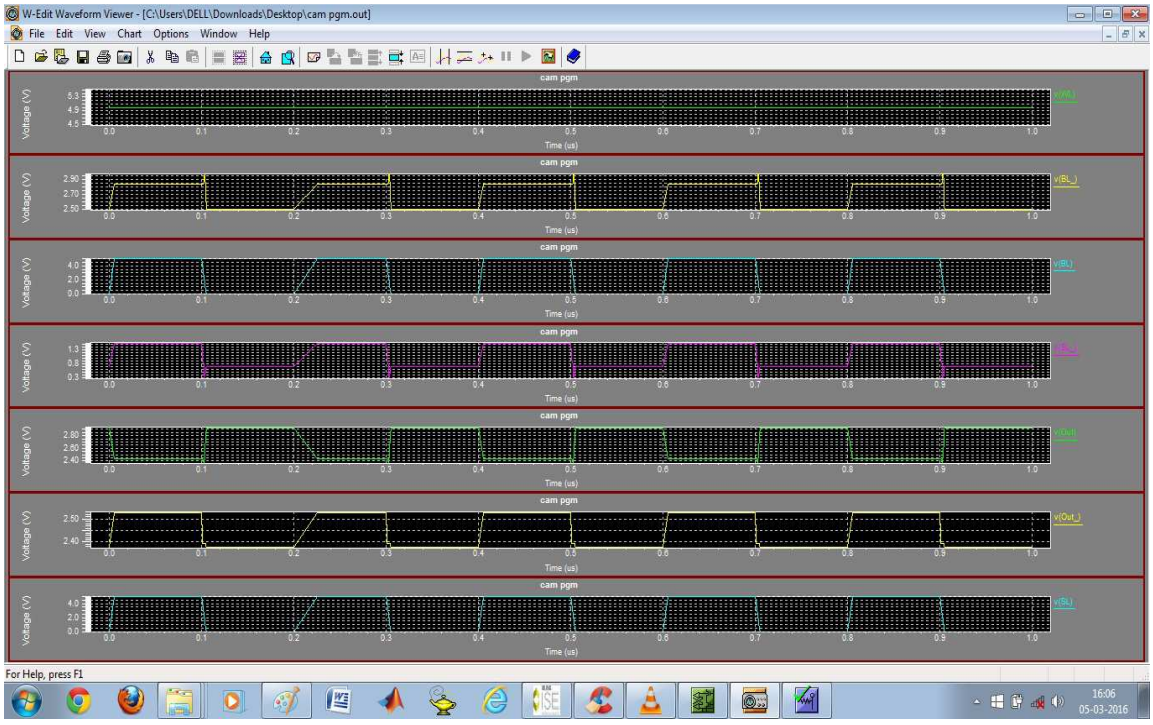


Fig.5.8 Output Waveforms of the NOR CAM bit cell using memristor and MT-CMOS in the W-Edit

COMPARISON OF OUTPUT

Fig 5.9 shows the comparison of power consumed at three different temperature

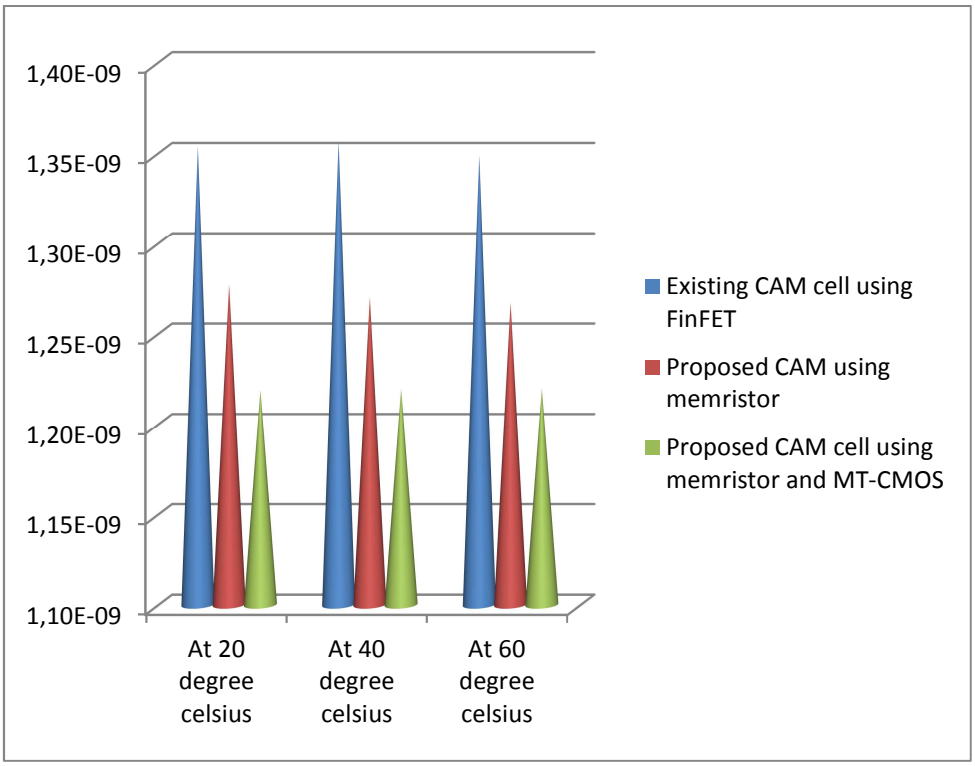


Fig.5.9 Comparison of average power consumed

6 CONCLUSION

The most important consideration in designing a device is less power dissipation and high performance. In this paper, An efficient design of Content Addressable memory using two elements namely, memristor and MT-CMOS has been presented. Because of the inclusion of memristor in the circuit, the CAM becomes non-volatile i.e. holds the data even when the device is not powered. This non-volatile property is nowadays an important consideration. Also, the usage of MT-CMOS reduces the leakage power which in turn reduces the average power consumed. Thus , a low power design of CAM is proposed and the design is drawn in S-Edit of Tanner EDA and output waveforms are seen in W-Edit and the average power consumed is measured. From the report obtained in T-spice. The graph showing comparison of the average power consumed in existing and proposed CAM is drawn. Thus, there is a significant reduction in the average power consumed. If a low power design of CAM is required, then the same circuit can be implemented in any of the logic styles of adiabatic logic using FinFET technology.

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