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A Novel Double Gate Tunnel FET based Flash Memory

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ABSTRACT: In this paper, a low power double gate TunnelFET (DGTFET) based flash memory cell is designed and its performance is studied through TCAD simulation. A DGTFET is converted into memory cell using floating gates. Its programming, erasing and reading operations are studied in the independently driven double gate (IDDG) mode through transient simulations. Out of the two gates one gate is used for "programming/Erasing" and the other gate is used for controlling the device characteristics dynamically and an application of a DC voltage to this gate reduces the reading delays.

KEYWORDS: Tunnel FET, Flash memory, Double gate, IDDG.

1 INTRODUCTION

Fundamental limitation on the sub-threshold performance is seen in bulk MOSFETs, SOI MOSFETs and FinFETs because of their drift –diffusion carrier transport mechanism. TunnelFETs (TFET) have been introduced to conquer this limitation. Since the charge transport mechanism is different, TFET's sub-threshold slope can be low compared to the conventional drift-diffusion-based devices. The drive current (I_{ON}) achieved by TFETs are low compared to conventional devices hence it has the popularity as the low power devices [1]-[4]. Nowadays, the flash memory technology is developing in a higher rate due to the tremendous growth in the digital consumer applications, such as mobile phones and digital cameras [5]-[6]. To reduce the short channel effects, we are going for multigate structure such as double gate FinFETs, in which the gates can be simultaneously driven or independently driven. Both the gates receive the same gate voltage in the simultaneously driven double gate (SDDG) whereas in the independently driven double gate (IDDG) the gates can be biased individually. In the IDDG devices the threshold voltage of one gate can be modified by varying the voltage on the other gate [7].

TFET based flash memory is a promising structure for ultra-scaled and low power flash memory application as explored in reference [5].TFET based flash memory with high-gate injection efficiency is proposed and experimentally demonstrated in reference [6].

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To the best of our knowledge, low power double gate flash memory in TFET is not realized so far. In this paper, the double gate flash memory is realised in TFET using TCAD simulations. The programming, erasing and reading operations are studied in IDDG mode through transient simulations. IDDG operation is studied in this device to get the dynamic threshold voltage of the device. The parameters, ON current (I_{ON}), OFF current (I_{OFF}) and threshold voltage (V_{TH}) are calculated for programmed and erased states.

Rest of the paper is organized as follows: Simulator models and the device structures are given in section 2. Device characteristics and results are discussed in the Section 3. Conclusions are provided in the final section 4.

2 SIMULATION

Sentaurus TCAD simulator from Synopsys is used to perform all the simulations. This simulator has many modules and the following are used in this study.

- Sentaurus Structure editor (SDE) : To create the device structure , to define doping, to define contacts,and to generate mesh for device simulation
- Sentaurus device simulator (SDEVICE): To perform all DC, AC and noise simulations.
- Inspect and Tecplot: To view the results.

Simulator includes the following models in the device simulation: oldslotboom of band gap model, Masetti of mobility model, nonlocal band-to-band (BTB) tunneling model combined with Shockley–Reed–Hall recombination and drift–diffusion physics [8].

Low power double gate TunnelFET (DGTFET) based flash memory structure is generated from SDE and is shown in Fig.1 with important parameters named. Table 1 gives the dimensions of the device.

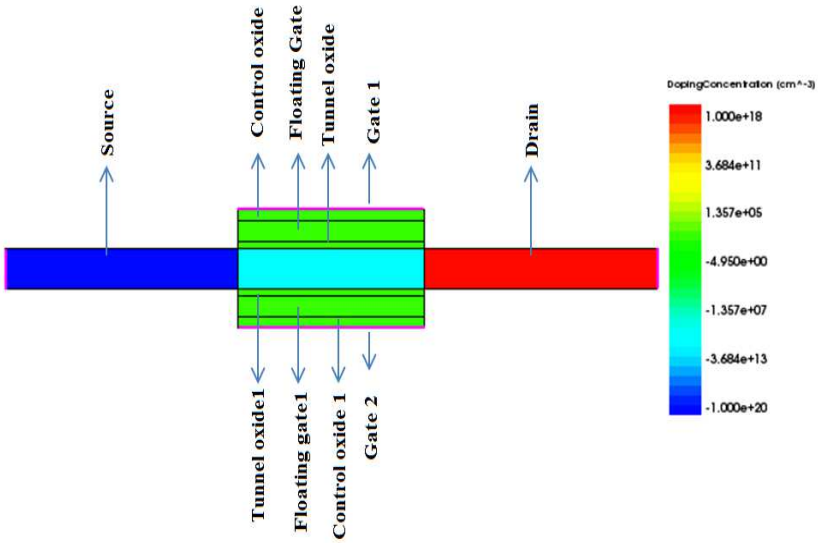

Fig.1 Structure of DGTFET Flash Memory

TABLE1. Device dimensions of DGTFET Flash memory

Parameter name	Value
Gate length	50nm
Width	10nm
Control oxide thickness	3nm
Tunnel oxide thickness	1.8nm
Floating gate thickness	5nm
Source doping (Ns)	$1x10^{20}$atoms/cm^3
Drain doping (Nd)	$1x10^{18}$ atoms/cm^3
Channel doping (Na)	$1x10^{17}$ atoms/cm^3

3 RESULTS AND DISCUSSION

Typical flash memory cell uses a floating gate to store a bit by the presence or absence of a charge. The results discussed in this section includes: the programming, erasing and reading operation for this DGTFET flash memory in IDDG mode. Gate1 voltage of 10V is used for programming, and -16V is used for erasing operations with the drain, source and gate2 are given with zero bias. Gate2 is used for modulating threshold voltages of the device while reading operation. The schematic view for erasing, programming states is shown in Fig. 2(a) and Fig. 2(b) respectively. Figure 3(a) and 3(b) show the space charge for programmed and erased states respectively. It is observed from Fig. 3(a) & 3(b) that the space charge is -1.37992x10^{20}(C/cm^3) for the programming state and is 3.2427x10^{20} (C/cm^3) for erased state.

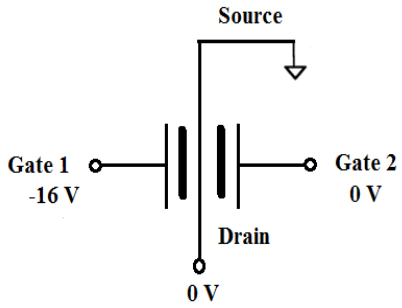

Fig. 2 (a) Schematic view of DGTFET Flash memory for erased state

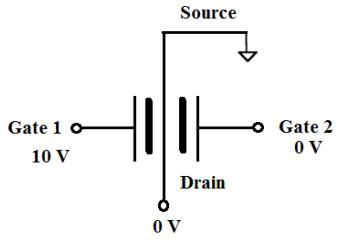

Fig.2 (b) Schematic view of DGTFET Flash memory for programmed state

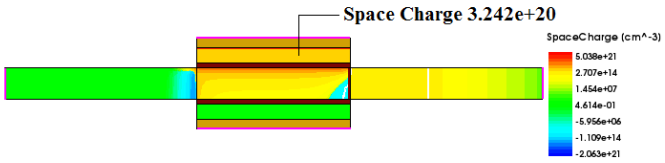

Fig.3 (a) Space charge structure of DGTFET Flash memory for Erased state

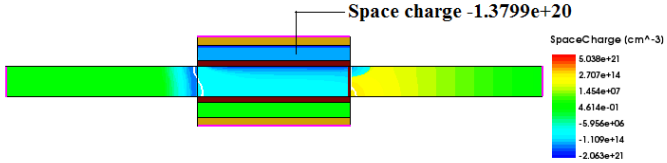

Fig.3 (b) Space charge structure of DGTFET Flash memory for Programming state

IDDG OPERATION

For reading operation, +3.25 V is applied to the gate1 of DGTFET Flash memory with the supply voltage as shown in Fig.4. The gate 2 voltage is varied from 0 to 1V for IDDG mode operation. I_D-V_G characteristics are done for reading operation.

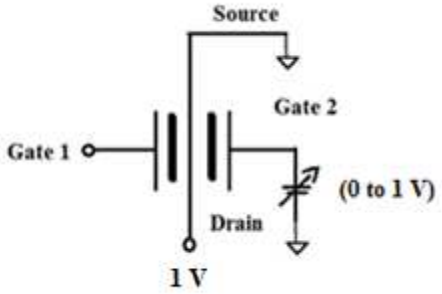

Fig.4 Schematic view of IDDG mode DGTFET Flash memory

Due to the increase in gate1 voltage the barrier in channel region is pushed down and the distance between valence band of Source to conduction band of channel is reduced. Hence the electrons in the valance band tunnel through the barrier into the conduction band of the channel and current starts to flow from source to drain. Figure 5 shows the OFF state band diagram of DGTFET Flash memory with zero bias given at both the gates. Fig 6 shows the ON state band diagram with gate1 voltage applied. It is observed from Fig.5 that there is no tunneling takes place from source to the channel, hence the device is in OFF state. Fig. 6 depicts the tunneling mechanism from the source to channel, hence the current flows from source to drain.

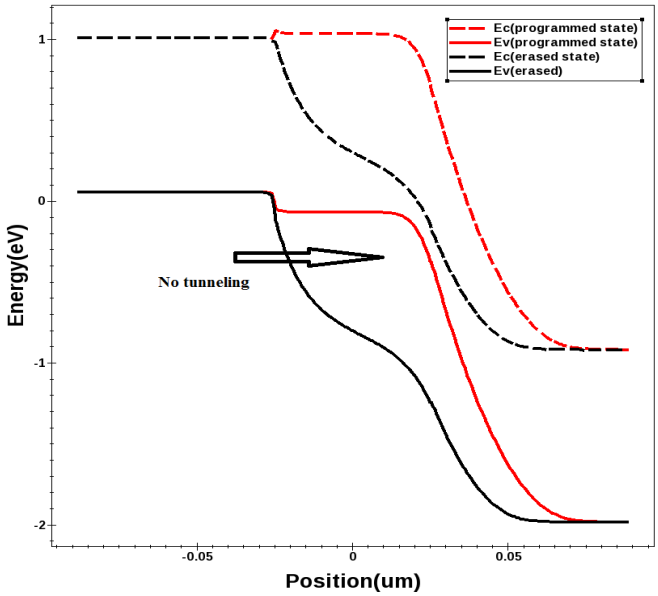

Fig 5 OFF state band diagram of DGTFET Flash memory

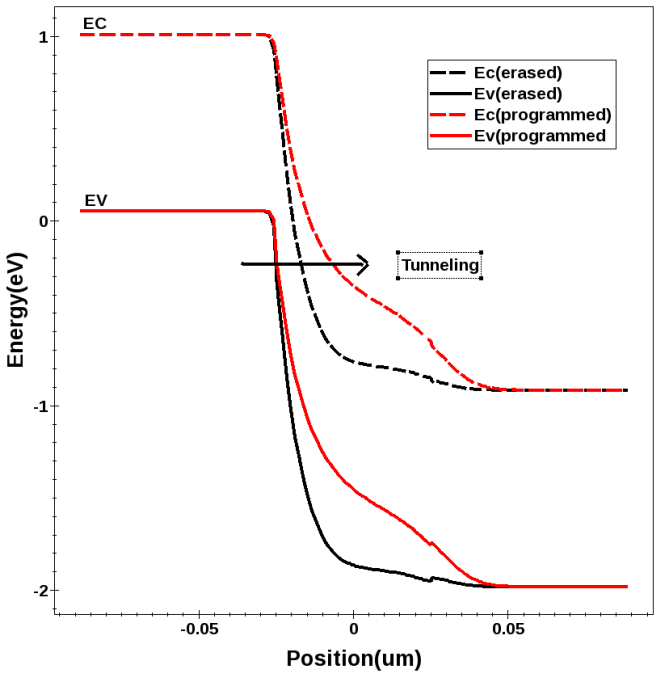

Fig 6 ON state band diagram of DGTFET Flash memory

The ON current (I_{ON}), OFF current (I_{OFF}) and threshold voltage (V_{TH}) are extracted from the I_D-V_G characteristics from Fig.7. As said earlier, the gate1 and gate 2 are biased independently in the IDDG operation. During the reading operation in IDDG mode, desired threshold voltage of the device is achieved. The reduction of threshold voltage will increase the I_{ON} and hence reduce the reading delay for both programming and erasing states.Figure.8 shows the energy band diagram for various gate2 control voltages. It is observed from Fig.8 and Fig.9 that the barrier width between Source to channel is getting reduced when the gate2 control voltage is increased. Hence the threshold voltage and reading delay also changes accordingly as shown in Table 3.

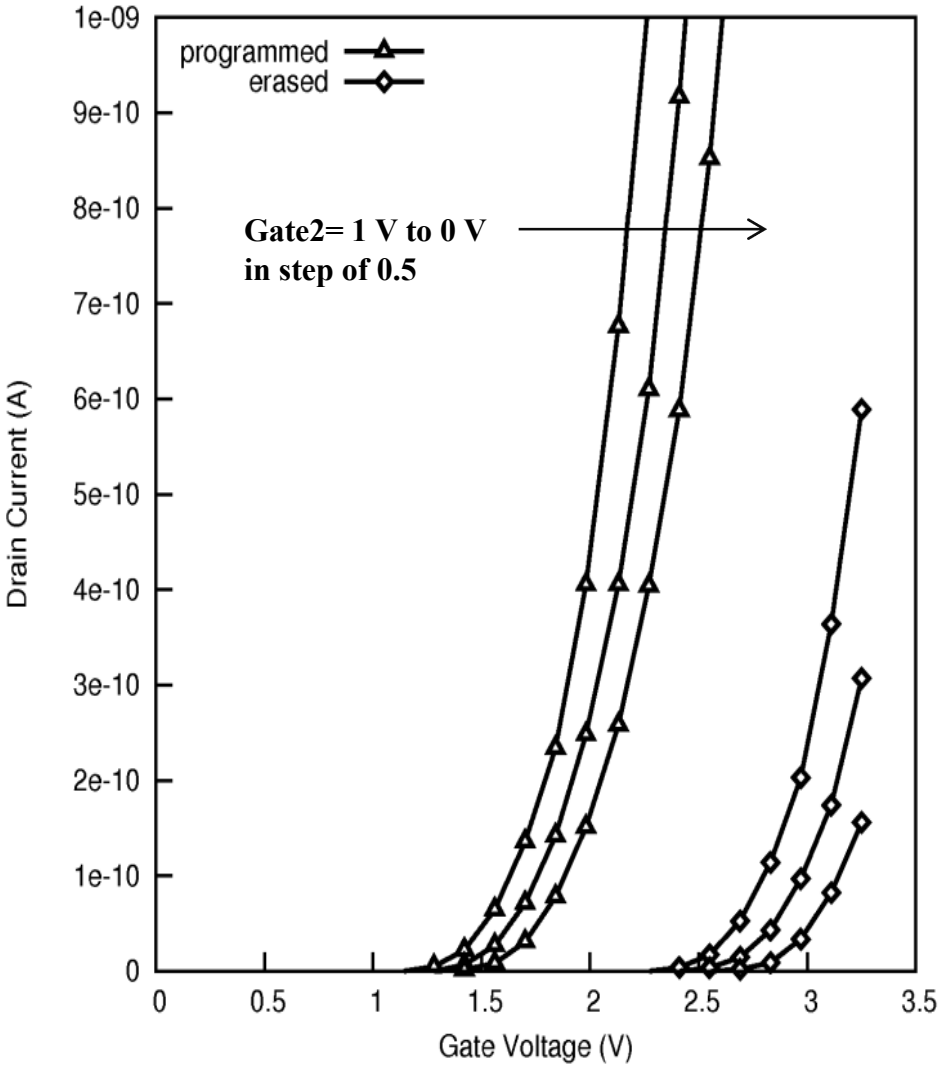

Fig 7 I_D versus V_G for various gate 2 voltages of DGTFET Flash memory.

TABLE.3 Reading Operation

GateVoltage (V)	Reading operation			
	Programmed state		Erased state	
	V_{TH} (V)	Delay(s)	V_{TH} (V)	Delay(s)
0	2.952	3.58e-11	2.543	3.60e-11
0.5	2.926	3.53e-11	2.569	3.56e-11
1	2.882	3.22e-11	2.567	3.48e-11

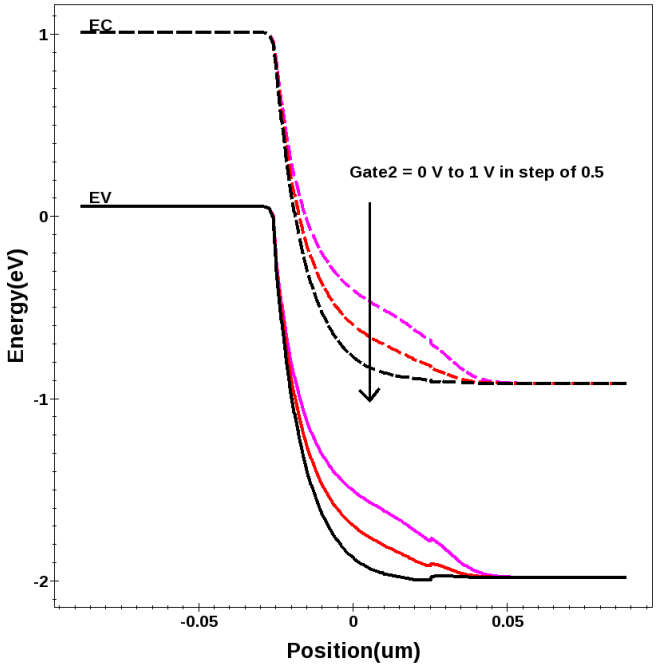

Fig 8.ON state band diagram for programmed state of DGTFET Flash memory

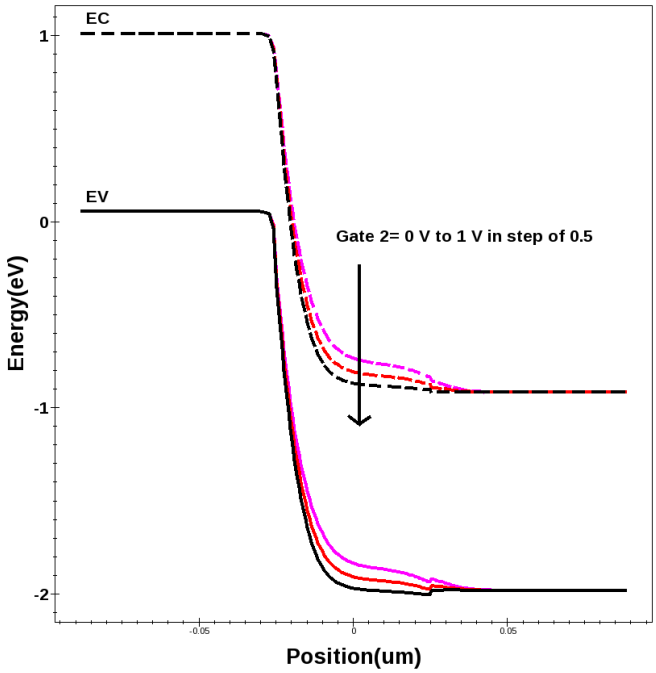

Fig.9 ON state band diagram for Erased state of DGTFET Flash memory

4 CONCLUSION

We have investigated the low power double gate TunnelFET (DGTFET) based flash memory cell through TCAD simulation. DGTFET flash memory's programming, erasing and reading operations were studied in the independently driven double gate (IDDG) mode. The parameters I_{ON}, I_{OFF}, V_{TH} were extracted in the IDDG mode for this device. The desired threshold voltage gate1 was achieved by adjusting the gate2 voltage by which the reading delay in programming and erasing states are reduced.

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