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Study and Fabrication of Crystalline Silicon Solar Cell in Bangladesh; Using Thermal Diffusion Technique

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ABSTRACT: The conversion of sunlight into electricity using solar cells system (10-14%) is worthwhile way of producing solar energy. The rapid fall in solar cell prices leads researchers to intensify their research on efficiency improvement of solar cells and to further reduce the costs of the fabrication process. Bangladesh receives strong sunshine throughout the whole year (3.8-6.42 Kw-hr/m^2) and it has been found that the average sunshine hours are 6.69, 6.16 and 4.81in winter, summer and monsoon, respectively. Bangladesh has good prospect of converting this sunlight into electricity through solar system, but there is no technology developed to fabricate solar cell locally in our country. To introduce this technology first time in Bangladesh "Bangladesh Atomic Energy Commission" has set up a laboratory to fabricate and research on crystalline silicon solar cell. This paper presents a solar cell fabrication process, in our solar cell fabrication laboratory, starts with a 200µm thick p-type silicon wafer using a diffusion technique with phosphorus oxy-chloride ($POCl_3$) gas source and metallization with screen printer. The resulting solar cell is mono-facial and it is fabricated using phosphorous diffusion and screen printing technique. Initially the efficiency of our fabricated solar cell was very low because it's very sensitive and depends on various parameters. The best achieved efficiency of our fabricated solar cell, using a screen printed and firing through metallization, on 161 cm^2 (total area) silicon wafers was about 7.0 %.

KEYWORDS: Solar energy, Fabrication process, Silicon wafer, Mono-facial, Phosphorus diffusion, Efficiency.

1 INTRODUCTION

The government of Bangladesh has declared that it aims to provide electricity for all by the year 2021 [1]. Energy is a critical input parameter for national economic development but Bangladesh has facing a power crisis for about a decade [2]. All the conventional sources of energy like gas, coal, oil etc. are limited. Currently most power plant in Bangladesh (represent 84.5% of the total installed capacity) use natural gas, the main commercial primary energy source with limited national reserves [2]. In this situation solar energy may be the sources of an alternative energy generation system. The location of Bangladesh is ideal for tapping solar energy effectively. Daily solar irradiation intensity varies from 3 to 6.5kW/m2, with a maximum during March-April and a minimum in December-January [3], [4]. More than 65,000 solar home systems are now being installed every month and about 3.5 million SHSs have already been installed which provides solar electricity around 09% of the total population of Bangladesh [5]. Though there is a vast demand of solar cell but no technology developed to fabricate solar cell in our country as a result the whole cells are imported from abroad. For the first time in Bangladesh we fabricate mono-crystalline silicon solar cell. There is a large variety of solar cell structures proposed with various types of materials, of which p-type Si solar cell has been one of the most popular and widely used in commercial production [6]. The

rapid fall in module prices leads researchers to intensify their research on efficiency improvement of solar cells and to further reduce the costs of the fabrication process [7]. For mono-crystalline silicon solar cell fabrication, phosphorous diffusion technique is the most widely used technique for photovoltaic industry [8]. The fabrication process of our Si solar cell starts with a 200µm thick p-type silicon wafer using a diffusion technique with phosphorus oxy-chloride (POCl3) gas source and metallization with screen printer. The efficiency of first fabricated mono-crystalline silicon solar cell was very low (0.8 %) but optimizing the instrument setup, develop some new technique and increase the skill of researcher we finally achieved 7% efficiency.

PRINCIPLE OF SOLAR CELL

Silicon solar cells consist of two essential steps. First, absorption of light generates an electron hole pair; second the electron and hole are then separated by the structure of the device electrons to the negative terminal and holes to the positive terminal thus generating electrical power [9]. Thus solar cell is an electronic device that produces electricity by directly converting energy from sunlight [10]. In order to construct a solar cell a p-n junction needs to be formed inside a semi-conducting material. The p-n junction makes a barrier which is known as the depletion region with a minor current and a very small amount of voltage (generally 0.1-0.3V) [11]. These small amounts of voltage create electric fields which play the vital role of solar cell operation. When sunlight is absorbed by the solar cell, as shown in Fig. 1, it will dislodge an electron, creating an extra mobile electron and extra mobile hole [12]. The electric field, created by the p-n junction, makes the electron flow to the N-type region and the hole flow to the P-type region. This is known as photo-generation of charge carrier and occurs throughout the N-type and P-type region. The resulting separation of negative and positive charges across the junction is called a potential difference or voltage.

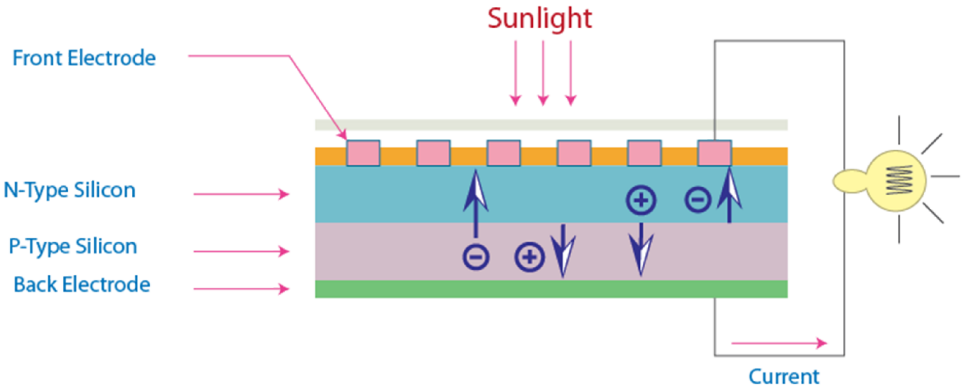


Fig.1. Solar Cell Operation

Connecting the solar cell is to an external circuit allows electrons and holes to travel round and recombine, resulting the system to its starting condition. The charges driven round the circuit from an electric current and do useful work such as lighting a bulb or one can storage this charge into a battery for further use.

2 FABRICATION PROCESS OF SILICON SOLAR CELL

The majority of silicon solar cell production is currently based upon a very standardized process that is intended to make a p-n-electrical junction on the entire front surface of the wafer and a full-area aluminum-based metallization on the back [13]. The fabrication process of our Si solar cell starts with a 200µm thick p-type silicon wafer. The wafers generally have micrometer sized surface damages that need to be removed. Figure 2 shows the steps of our silicon solar cell fabrication process. After the saw damage removal, the wafer surface shows high optical reflectivity, for which the top surface was textured by chemical etching before emitter diffusion. After cleaning and texturing, the edge isolation was carried out, as otherwise the top and the bottom surfaces of the wafers remain electrically shorted.

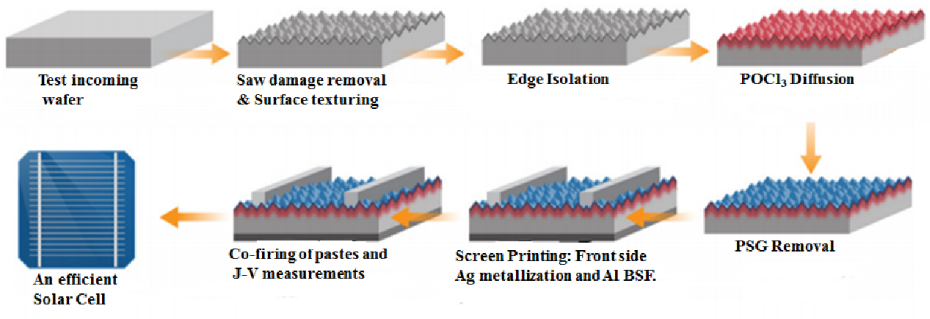


Fig.2. Steps of solar cell fabrication process.

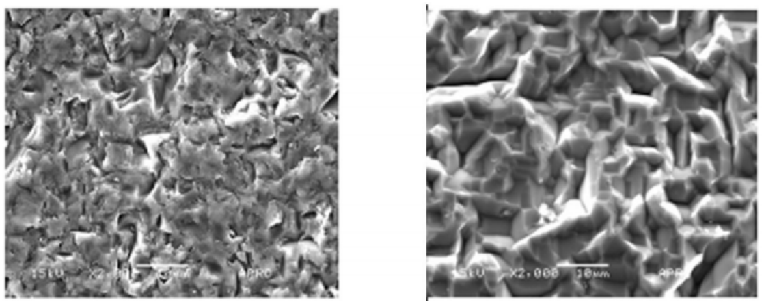
For a p-type silicon wafer, an n-type top layer acts as emitter. A thermal diffusion is commonly used for emitter diffusion [14]. After emitter diffusion, an electrical connection to the cell becomes necessary to operate the solar cell. Ag and Al metal electrodes were formed by using screen printing of silver and aluminum pastes and co-firing at a suitable temperature.

2.1 TEST INCOMING WAFER

First, because wafers are typically received from multiple supply sources, and because they can be damaged during sawing and shipping, all incoming wafers should be tested to ensure that they would provide a foundation for acceptable cell efficiencies [15]. Specifically, for the purposes of wafer metrology, measurements of the minority charge-carrier lifetimes would be quite informative [16]. With surface photo-voltage (SPV) measurement system by measuring of SPV as a function of wavelength, we calculate the minority carrier diffusion length and charge carrier lifetime. If the value is in acceptable limit then we accept the wafer to fabricate silicon solar cell.

2.2 SAW DAMAGE REMOVAL PROCESS

Saw damage removal process was done in wet chemical bench to remove the organic contaminants and to partially remove the micro-cracks from the silicon wafer surface that might compromise the wafer's resilience to breakage during handling in cell processing. The surface damages to the wafers were removed through isotropic etching with a concentrated solution of NaOH in de -ionized water (DI-W). DI-W helps the NaOH to break in Na+ and OH- ions in the solution. The 10% NaOH solution was make with 6 liter of DI water which was transferred to a clean beaker and then 600gm NaOH pellet was added to the beaker. After that the solution was heated and when it reached at 70°C temperature then dipped the silicon wafer into that solution for about 10 minutes for etching, which removes the surface damages. Figure 3 shows the Scanning Electron Microscope (SEM) image of saw damage surface wafer and saw damage removed and clean surface wafer. This cleans the wafer surface with an approximate silicon etching rate of 500nm/min [17].



(a). Untreated surface ***(b). Saw damage removed surface***

Fig.3. Comparison of SEM image of the (a) saw damaged wafer surface, unclean and (b) saw damage removed clean surface silicon wafer.

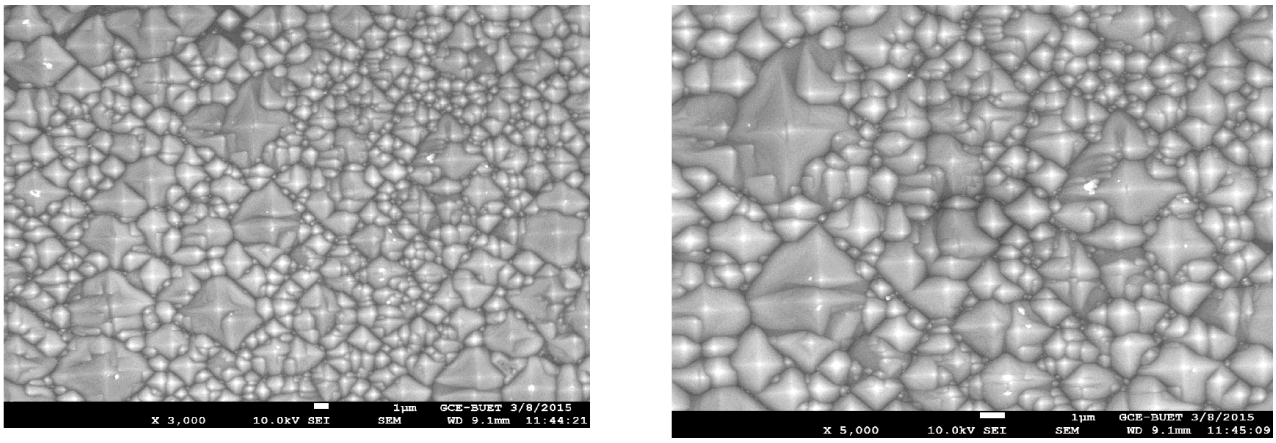
This saw damage removal step, etches out about 5 micro meter silicon from wafer surface. After that the wafers were rinsed in DI-W for 1 minute then dipped into the HF (02%) solution for 3 minute and finally again rinsed in DI-W for 1 minute.

2.3 SURFACE TEXTURING PROCESS

For this process, a wet bench chemical treatment was utilized to etch away between 5 and 15µm of silicon wafer from the top surface. The characteristics of the etching depend upon, time of etching, etching rate, temperature, components of the solution and its concentration. This is typically achieved by exposing the wafers to an aqueous solution of potassium hydroxide (KOH) with isopropyl alcohol (IPA) [15]. IPA enhances surface diffusion, so a rapid etching can take place in presence of IPA in the solution [18]. With the alkali metal only being a spectator ion, the etching reaction proceeds as follows [19]:

$$Si + 2KOH + H_2O \longrightarrow K_2SiO_3 + 2H_2$$

The potassium silicate (K_2SiO_3) is soluble in water and thus silicon surface remains devoid of any deposition. For texturing process, we prepared a solution using the ratio of, KOH: IPA: H_2O = 1 gram: 5 ml: 125 ml. Initially 6 liter of DI water was transferred to a clean beaker and then 48gm KOH pellet was added to the beaker. The solution was then heated and when it reached at 70°C temperature, we dipped the silicon wafer and added 240 ml of IPA into that solution. After 10 minutes the wafers ware removed from the beaker and rinsed with DI-water then the hydrophobic process was repeated and finally the wafers ware dried using the compressed air. The etch rate of this chemical reaction is different for different crystallographic orientations. The anisotropic etchants is expected to etch (110) plane at a faster rate than the (100) plane while the (111) plane etches at a slowest rate [20]. Due to these anisotropic differences in etch rates the originally flat wafer surface was etched into morphology of pyramids having a random distribution in size. Figure 4 shows the Scanning Electron Microscope (SEM) image of a textured wafer. Fortuitously, these pyramids can provide the foundation for front-surface light trapping [21].



(a). 3,000 times magnification *(b). 5,000 times magnification*

Fig.4. SEM image of textured silicon wafer

At the conclusion of this wet bench chemical processing step the wafer is then ready for the formation of the topside p-n electrical junction.

2.4 EDGE ISOLATION PROCESS

The edge isolation was carried out after screen printing of acid barrier paste as a mask, by the reactive ion etching [22-23]. The purpose of the edge isolation treatment was to separate front side and back side, as otherwise the top and the bottom surfaces of the wafers remain electrically shorted. In our process back side of the wafer edge was masked using a screen printing machine and a diffusion barrier paste was used to isolate the edge. Figure 5 shows the designed screen which was used in our experiment.

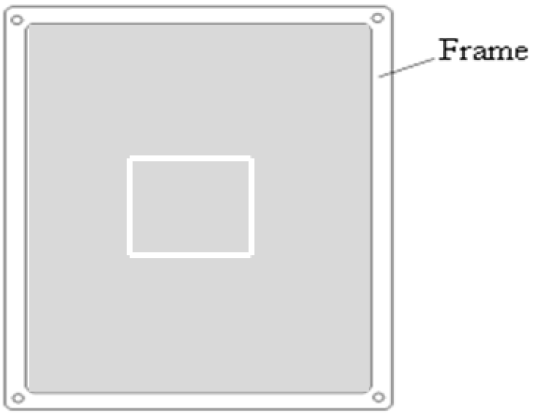


Fig.5. Image of screen used for wafer edge isolation

After the screen printing, the printed wafers ware dried for 10 minutes in a preheated oven at 120°C.

2.5 PHOSPHORUS DIFFUSION PROCESS

The standard silicon solar cell is generally made with a boron doped (p-type) base wafer. For this p-type silicon substrate, an n-type top layer acts as emitter. A thermal diffusion is commonly used for emitter diffusion [14, 24]. The thermal diffusion of phosphorus is necessary to create an n-type emitter to the p-type wafer [25]. Phosphorus (P) diffusion is currently the primary method for emitter fabrication in silicon (Si) solar cell processing [26] [27]. Along with nitrogen (N2) and oxygen (O_2) gases, phosphorus oxy-chloride ($POCl_3$), a liquid source of phosphorus, is also widely used in the standard diffusion process of solar cells [28], [29].The diffusion depends on various factors, of which temperature and gaseous environment is most important [30]. In oxygen environment and at high temperature, phosphorus diffusion leads to formation of n+ type emitter at the top surface of the wafer. The diffusion was carried out in two stages, pre-deposition and drive-in [31], [32]. The formation of phosphorous-rich oxide films, phosphosilicate glass (PSG), on the silicon substrate carry out at pre-deposition stage and in drive-in stage, the phosphorous-rich oxide film acts as an infinite source for phosphorous diffusion into the Si substrate. The phosphorus atoms formed at the PSG-Si interface penetrate through the silicon wafer [27] and can be simplified with the following reaction equations:

$POCl_3$ (liquid) + N_2 (bubble) → $POCl_3$ (vapor) (pre-deposition)

4 $POCl_3$ + 3O_2 →2 P_2O_5 + 6 Cl_2

2 P_2O_5 + 5Si →4P + SiO_2 (drive-in)

P + 3Si → n-type doped Si

For emitter diffusion we were used a quartz tube in a heated horizontal furnace, a diffusion furnace, and first the tube temperature was set to 600 °C. Once the temperature reached 600°C, the quartz boat containing the wafers were slowly moved into the middle of the diffusion chamber so that the wafers do not suffer large temperature gradients and warping. Then nitrogen gas was turned on and waits for 10 minutes and then increased the tube temperature from 600°C to 875 °C keeping the nitrogen gas on. After that, nitrogen gas was turned off and oxygen and $POCl_3$ (Phosphorus oxy chloride) were turned on simultaneously when the tube temperature reached at 875 °C and wait 10 minutes to activate the diffusion of phosphorous into the wafer. After 10 minutes of diffusion time oxygen and $POCl_3$ gas ware turned off simultaneously and nitrogen gas was turned on and we have to allow the nitrogen gas to flow for 10 minutes in the quartz tube so that no other gas is present in the tube. After 10 minutes nitrogen gas was turned off and only oxygen gas was turned on for the next 10 minutes so that phosphorus atoms from the n+-type top layer diffuses deeper into the wafer, forming a deeper junction. Then the oxygen gas was turned off and nitrogen gas was allowed to flow for 10 minutes, finally the temperature of the chamber was reduced to 600 °C from 875 °C and during this stage nitrogen gas was kept turned on. Once the temperature of the chamber dropped to 600 °C, the nitrogen gas was turned off and the wafers ware take out for the next stapes. Figure 6 shows the phosphorus doped silicon wafer.

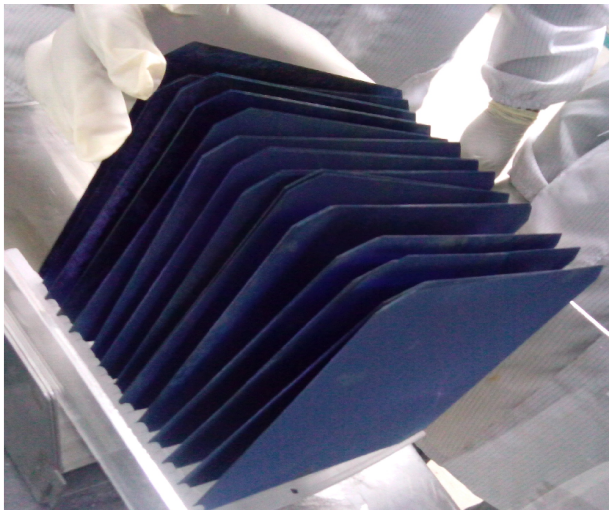


Fig.6. phosphorus doped silicon wafer.

2.6 PHOSPHOSILICATE GLASS (PSG) REMOVAL

In presence of oxygen, phosphosilicate glass (PSG) is formed at the 850°C temperature. Phosphosilicate glass or PSG is phosphorus doped silicon dioxide, a hard material layer formed at the top surface of Si wafer in the pre-deposition stage of diffusion process [25]. In the drive-in stage, a deeper junction was formed as phosphorus atoms from the PSG layer diffuse deeper, thus thicker emitter and a lower surface concentration of dopant was achieved. But a thin PSG layer was still present on top of the wafer after drive-in stage of diffusion. Due to this thin phosphosilicate glass (PSG) layer the top wafer surface becomes glassy and degrade blue response of solar cells. To remove the PSG layer we prepared a 10% hydrofluoric acid (HF) solution and then dipped the silicon wafer for one minute after that the wafer were rinsed with DI-water.

2.7 FRONT AND BACK SURFACE METALLIZATION PROCESS (SCREEN PRINTING)

To form electrical contacts on the front and back side of solar cell, metallization process was done using screen printing method. Screen-printing (SP) is cost effective, robust, simple, inexpensive, and fast method of metallization of the solar cells [33-34]. The screen printing of Ag and Al pastes for the formation of the front and rear electrical contacts has been in use by the silicon industrial community since the 1970s [35]. At the front surface the metallization creates electrical connection to thin n+ layer whereas at the back surface it provides an electrical connection and at the same time it creates a p+ layer. The solder paste that used in this work was Ferro FX53-038, aluminum type for rear surface while for the front surface, Ferro CN33-462, silver type was used. We use specific type screen mask to screen print of front and back side of solar cell. This screen is made up of an interwoven mesh kept at a high tension, with an organic emulsion layer defining the printing pattern. Figure 7 shows a microscopic image of the screen and the screen mask which was used for front side printing. An H-pattern screen that was mounted in an aluminum frame was then overlain on the front side of the cell and the metallization paste was squeegeed over the wafer surface with a screen printer.

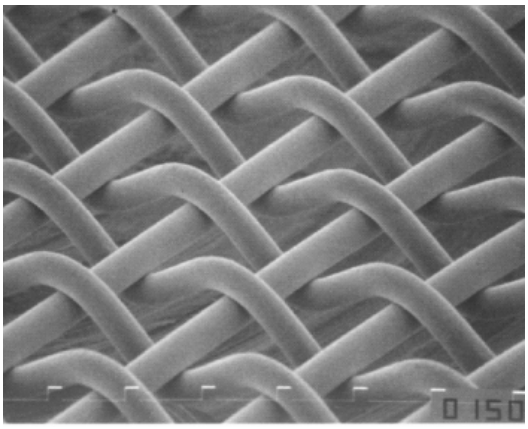
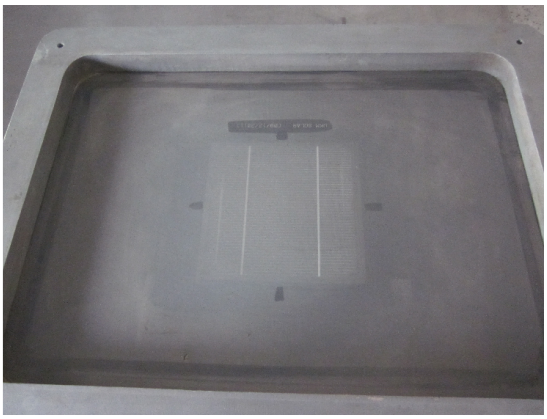


Fig.7. a) Microscopic image of the screen



b) Image of front side printing mask.

After the front-side screen-printing, the wafers are moved into a low-temperature (200 0C) drying oven, and the wafer was then moved on to another screen printer for the rear side printing with Al paste.

2.8 CO-FIRING PROCESS

Following screen printing, high temperature process was used to cure contacts in order to form ohmic contacts. The rapid thermal annealing (RTA) furnace was used to cure or fire screen printed contacts on silicon solar cells. It is one of the most sensitive steps of the solar cell fabrication [25]. Rapid thermal annealing is important because it provides proper contact between the conductor and the semiconductor of solar cell. A three temperature zones and one cooling zone annealing furnace with conveyer belt system was used in our co-firing process. The wafers were passed inside the RTA furnace through a moving belt with speed 60 inch per minute and figure 8 shows the contact firing process of screen printed Si solar cell. While during the rapid thermal annealing process, the cell was then fired with the general temperature profile and in our experiment it was 500, 600 and 800 °C for three temperature zones respectively.

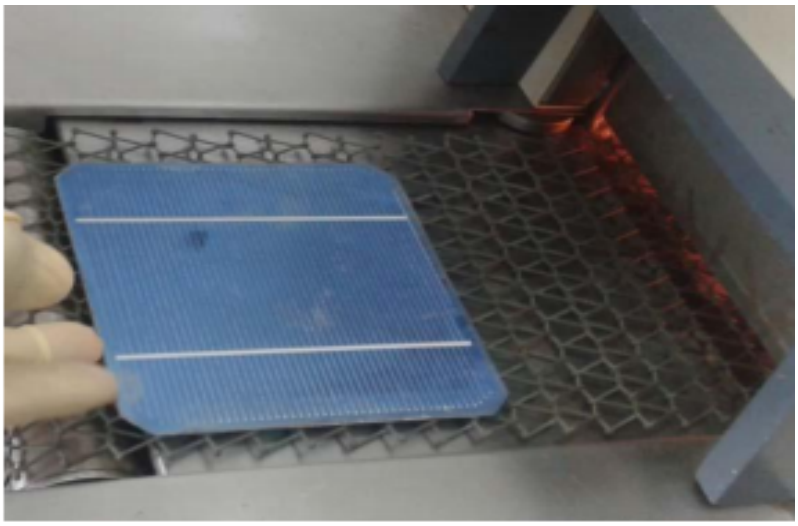


Fig.8. Contact firing of solar cell with RTA furnace

The first zone was the warming up zone so that the silicon wafer cannot experience a sudden temperature change. In the second and third zone the annealing take place while the last zone was cooling zone (before the wafers going out from the furnace). After contact firing the solar cell was then collect from the conveyor belt. Special heat protective gloves were used because all these things were done at very high temperature so safety has to be ensured.

2.9 CHARACTERIZATION (CURRENT-VOLTAGE MEASUREMENT)

After finishing a complete solar cell, some characterization tests were carried out. These tests show how efficient the solar cell was. The major characterization equipment was LIV tester with which it was possible to evaluate the performance of the cell and mainly to calculate the efficiency of the solar cell. The variables that also taken to consideration were the short circuit current (Isc), open circuit voltage (Voc), fill factor and cell power. The fabricated solar cell was tested under one-sun conditions using Xenon-arc lamps; a xenon spectrum is closest to sunlight [27]. Data acquisition based on programmable current-voltage source power supplies capable of handling currents up to 8A was used in conjunction with a proprietary data acquisition system. Calibration of this LIV measurements system was based on independently measured Si solar cells at Sandia National Laboratories. These LIV system was a user-friendly Lab View interface that capable of writing data, the LIV tester are shown in Figure 9, in ASCII format forms the basis of data acquisition.

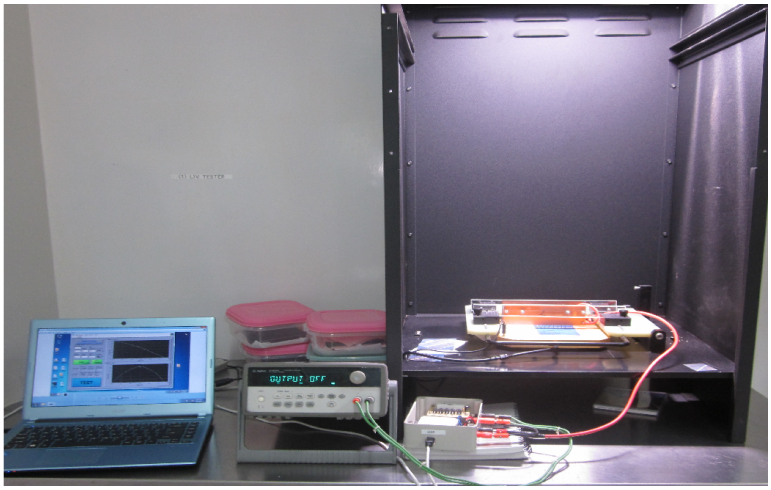


Fig.9. LIV Measurement System

3 RESULT AND DISCUSSION

In our fabrication process we were used 200µm thick p-type silicon wafer but thin silicon wafer was more economical because it consumes less Si material, and results in more efficient solar cell because of higher built in field. Cost of silicon was one of the major expenses in Si solar cell production and thus with less consumption of semiconductor mass in the form of thinner wafer, the cost of production can be significantly reduced.

Now-a-days it is seen that 'Spin on Dopant' method is cheaper than diffusion from a POCl3 source. In this process liquid dopant solution is applied to the wafer and the wafer is spun at high speed to produce a thin film source. But the main advantage of phosphorus diffusion technology was the self-governing control of the pre-deposition and the drive-in, due to which the surface source can more easily be made finite. Thus, a greater control of the surface concentration of phosphorus diffused emitters was achieved.

Resistance of screen printed front electrode provides additional element to the series resistance. Each electrode creates a shadow to the cell that reduces total number of electron-hole pair generation under constant illumination. Thus, although decreasing the spacing among the electrodes help reducing series resistance, yet shadow effect leads to reduced total number of electron-hole pair generation. For this, a finger with good conducting material and a high aspect ratio is preferable and only the 10% of total surface was covered with finger. The temperature profile during the rapid thermal annealing process is also influence the results of the produced cells so it was set very carefully.

After fabrication process, the completed solar cells were then tested using the Light I-V (Light-Current-Voltage) tester to evaluate the performance of the cell and mainly to calculate the efficiency of the solar cell. Figure 10 shows the output of LIV measurement system.

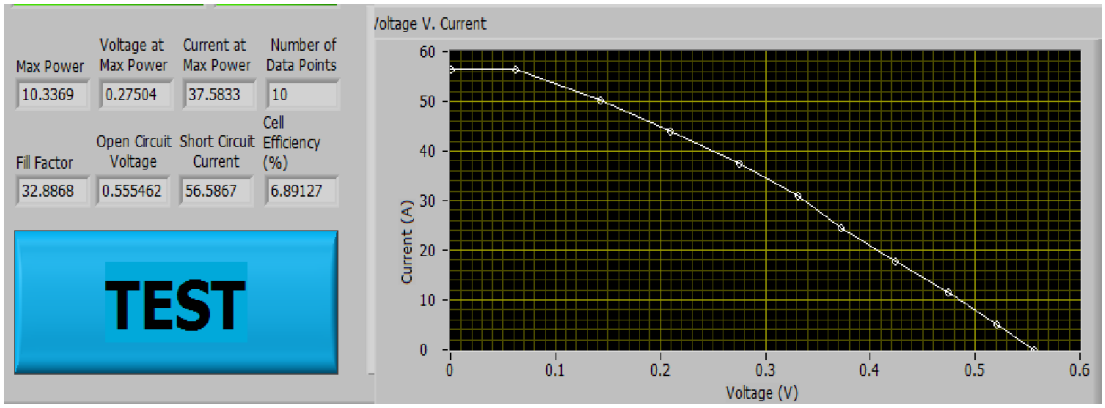


Fig.10. Measured LIV data

We have found the following results of our fabricated silicon solar cell which are, Maximum power was 10.3369W, Voltage at maximum power was 0.27504V, Current at maximum power was 37.5833mA, Open circuit voltage was 0.555462V, Short circuit current was 56.5867mA, Fill factor was 32.8868 and Efficiency was 6.89%.

4 CONCLUSION

The fabrication process of our Si solar cell starts with a 200μm thick p-type silicon wafer using a diffusion technique with phosphorus oxy-chloride ($POCl_3$) gas source and metallization with screen printer. The efficiency of our fabricated solar cell is about 7% which is quite low as compared to the commercially available solar cell in the market. But with this laboratory facility now it is possible to fabricate silicon based crystalline solar cell and to characterize local and imported fabricated cell which is a great technological progress for us in the field of solar energy. The efficiency of fabricated solar cell depends on various parameter, for instance cleaning and texturing process, optimum flow rate for $POCl_3$ and fixing the different temperature zones of RTA process is achieved which can significantly enhance the solar cell efficiency. Our main objective to develop the existing technology and innovate some new technology to fabricate cost effective high efficiency silicon solar cell that will help to solve our power crisis as well as improve our socio-economic condition in a great deal.

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