

A Low Noise Variable Gain Amplifier

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ABSTRACT: A Low noise variable gain amplifier (VGA) was designed using TSMC 0.13 um CMOS technology. This design is proposed to work at frequency range of 40 to 950 MHz. In this proposed work a numbers of attenuators are placed after two stages of Low noise amplifiers [LNA]. Each attenuator is used to obtain variable gain of amplifier. Control Voltage is applied to each attenuator to obtain variation in gain. The first stage of amplifier is designed for high gain and low noise figure. The second stage is designed for high gain and high linearity. The proposed VGA have achieved the gain of -0.81 db to 29.08 db at 40 MHz and -3.14 db to 26.644 db at 950 MHz. The noise figure of proposed designed is 1.747 db at 40 MHz and 1.411db at 950 MHz when all attenuators are off and 4.032 db at 40 MHz and 4.995 db at 950 MHz when all attenuators are on.

KEYWORDS: Low Noise Amplifier (LNA), variable gain amplifier (VGA), Attenuator, Linearity, Noise figure.

1 INTRODUCTION

Variable gain amplifiers (VGAs) are an important building block for to maximize the dynamic range of system like disk drives and wireless communication link [1]-[3]. There is a need to increase the bandwidth over a several tens of megahertz and at the same time it is required to decrease the power consumption for many multimodal applications [4]. The VGA has many advantages like low power consumption, continuous gain tuning and small chip size. The output linearity of the VGA can be improved by applying load degeneration technique [1]. There are two methods to build VGA, one analog controlled VGA [2] and other digitally controlled VGA [5]. In these design we are using analog controlled VGA. Variable gain amplifier (VGA) is implemented for high speed communication receiver system. In this a dc offset cancellation and dual feedback network for bandwidth extension method is used [6]. The variable gain amplifier (VGA) can be achieved by changing the gain transfer function of an amplifier according to the gain control signal. It also be obtained by continuous gain tuning in which a linear db gain is controlled and implemented [7] [8]. In order to control signal levels in the receiver, adjustable attenuators are useful. Particularly, a high linearity characteristic is a key requirement in most modern wireless communication [9]. In spite of all these, a different method using attenuator is implemented in the current paper. In this method, numbers of attenuator are placed after two stages of low noise amplifiers (LNA). Each attenuator are used to obtain variation in gain. So, by controlling the bits of attenuators variable gain of amplifier can be obtained.

3 DESIGN SCHEMATICS

Fig. 3. Shows the proposed design of low noise variable gain amplifier which is implemented in Agilent's ADS 2009 software. The first two stages are of amplifiers which are followed by the four stages of attenuator. Fig. 3. Shows the two stages of amplifier followed by an attenuator but in actual design a four stages of attenuators are used to obtain about 30db of attenuation. The first stage of amplifier is implemented for a high gain and low noise figure. Second stage is designed for high gain and high linearity. The stages of attenuator provides the variation in gain hence a variable gain amplifier is obtained. As we require high gain and low noise figure characteristics we are using a LNA, as the two stages of amplifiers. Both these parameters are trade off, so there were several topologies for broad band characteristics such as compensated matching theory and feedback method [9]. In these proposed design a self biased negative feedback topology is used. In these both the transistor M1, M3 forms a CMOS inverter with a negative feedback resistor. Using this method M3 transistor will adapt the same voltage level of M1 transistor and is called as self biasing and hence the same amount of current flows in M1 as well as in M3. The same LNA topology is used for the second stage. So we obtained a high gain, low noise figure and high linearity. Each Attenuator is placed after the amplifier to obtain the variation in gain. We are using the T pad attenuator topology. In this design of attenuator we are using MOS as a switch. By controlling on or off state of switch, variation in gain can be obtained. When VC1, VC3 and VC5 are on and VC2, VC4 and VC6 are off, then all the attenuators are off. When VC1, VC3 and VC5 are off and VC2, VC4 and VC6 are on, then all the attenuators are on. So by controlling the states of switch a variable gain amplifier is obtained. The four stages of attenuator are used to obtain 30 db attenuation.

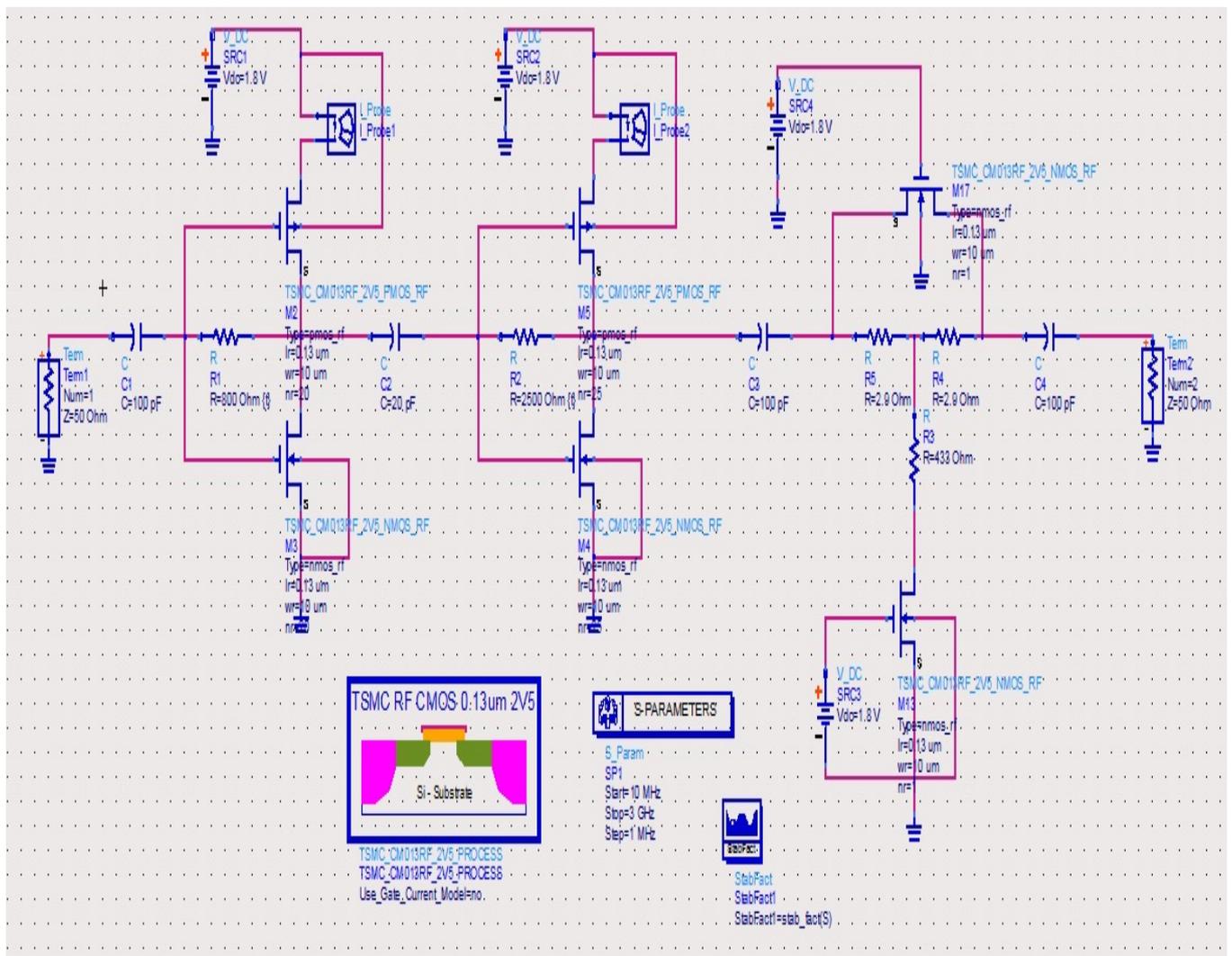


Fig. 3. Proposed design of variable gain amplifier

4 MEASUREMENT RESULTS

In this section the results of the proposed designed are shown. This section discusses Gain, Noise Figure and stability. The proposed design of VGA is obtained by using TSMC 0.13 um CMOS technology. This design is proposed to work at frequency range of 40 to 950 MHz

Fig. 4. Shows NF results when all attenuator are off. NF ranges from 1.747dB to 1.411dB for 40MHz to 950 MHz. Fig. 5. Shows NF results of VGA when all attenuator are on. NF ranges for 4.032 db to 4.995 db over the operating frequency range. So the noise figures of proposed designed of VGA ranges for 1.747 db to 4.032 db and for 1.411 db to 4.995 db over the operating frequency range.

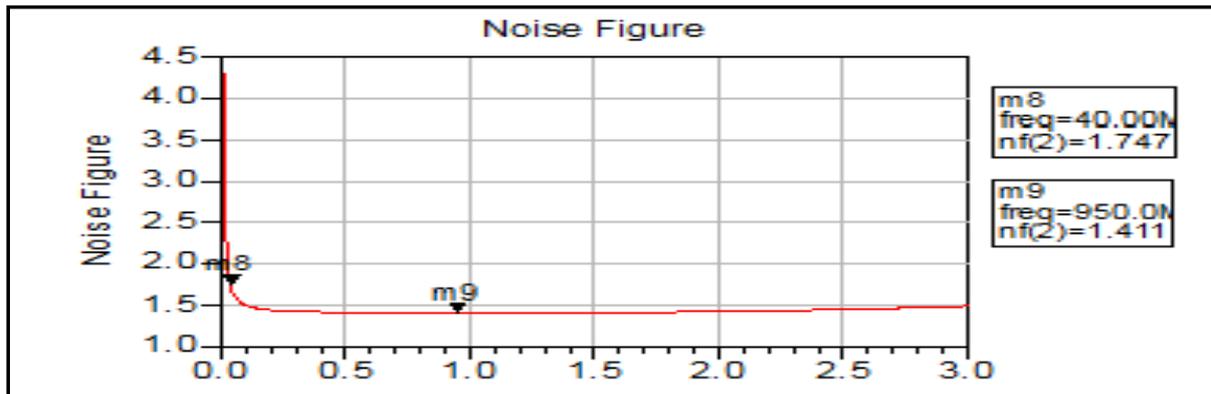


Fig. 4. Noise Figure over the operating frequency range when all attenuators are off

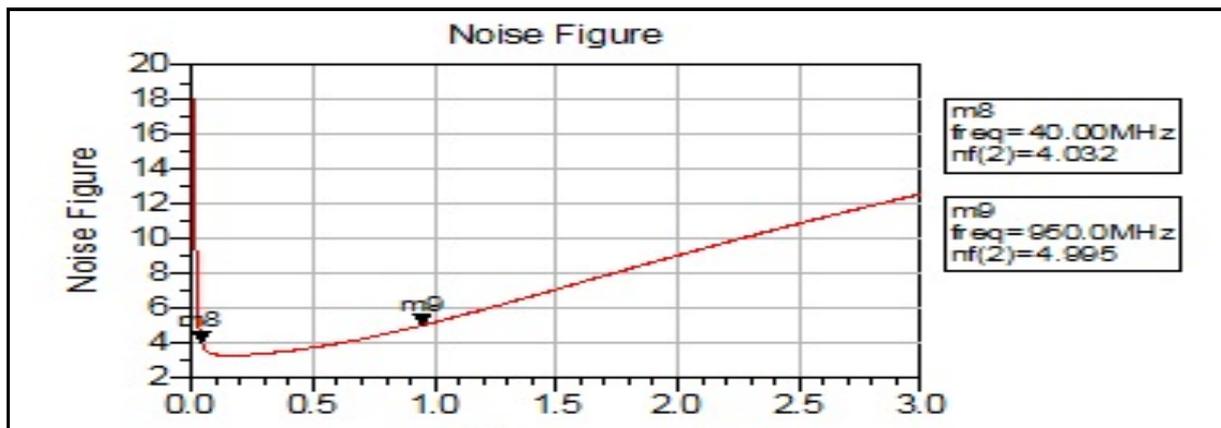


Fig. 5. Noise Figure over the operating frequency range when all attenuators are on

Fig. 6. and Fig. 7. Shows gain achieved by the proposed design. The proposed design achieved the gain of -0.81 db to 29.08 db at 40 MHz and -3.14 db to 26.644 db at 950 MHz, for variation in gain four stages of attenuator is used so we obtained an attenuation of about 30db. This attenuation is obtained by controlling the switch of attenuator.

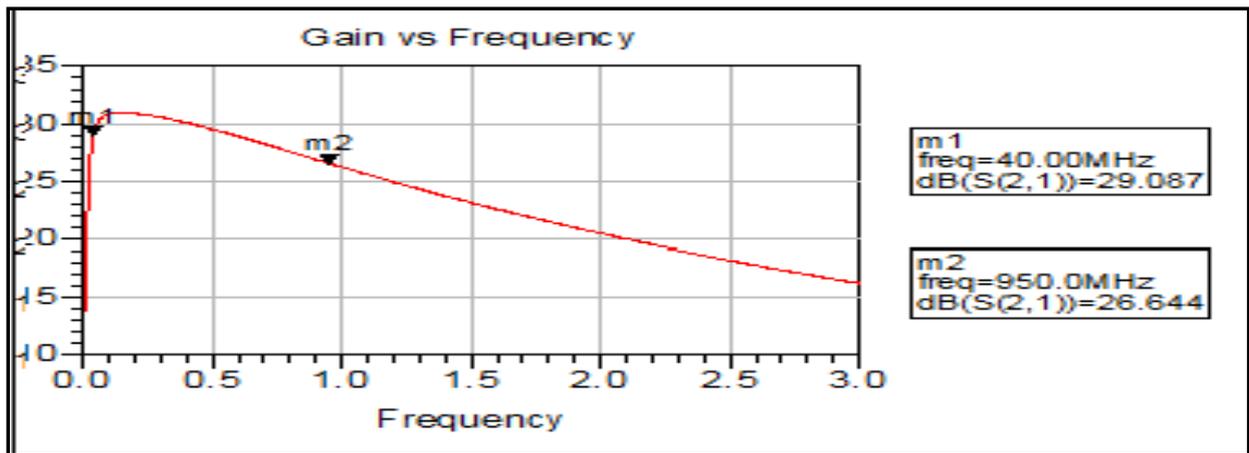


Fig. 6. Gain v/s frequency when all attenuators are off

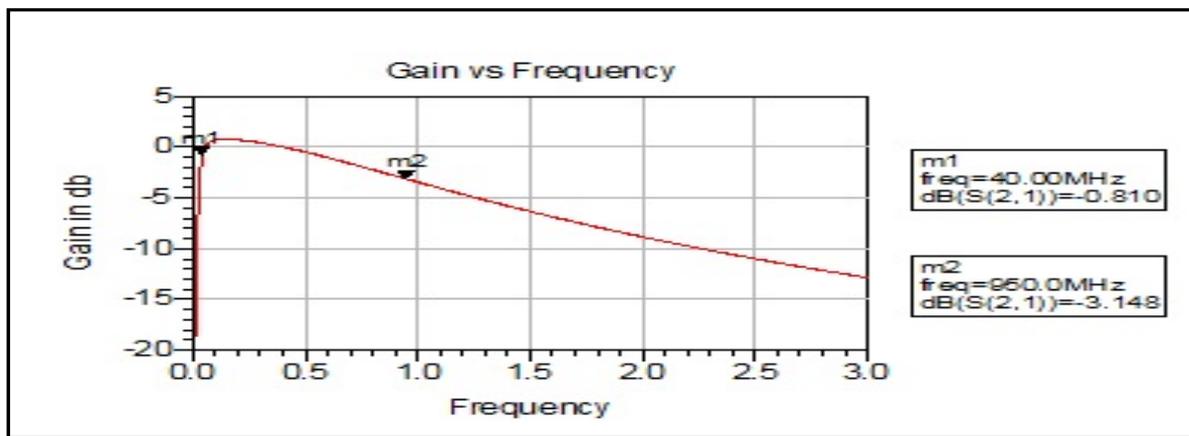


Fig. 7. Gain v/s frequency when attenuators are on

Table 1. Control strategies for VGA

VC1	VC2	VC3	Control Voltages					Gain		Attenuator status			
			VC4	VC5	VC6	VC7	VC8	40Mhz	950Mhz	first	Second	third	fourth
1	0	1	0	1	0	1	0	29.08db	26.644db	off	off	off	off
0	1	1	0	1	0	1	0	22.205db	19.839db	on	off	off	off
1	0	0	1	1	0	1	0	21.496db	19.109db	off	on	off	off
1	0	1	0	0	1	1	0	21.321db	18.911db	off	off	on	off
1	0	1	0	1	0	0	1	21.652db	19.216db	off	off	off	on
0	1	0	1	1	0	1	0	14.36db	12.016db	on	on	off	off
0	1	0	1	0	1	1	0	6.627db	4.288db	on	on	on	off
0	1	0	1	0	1	0	1	(-)0.810db	(-)3.14db	on	on	on	on

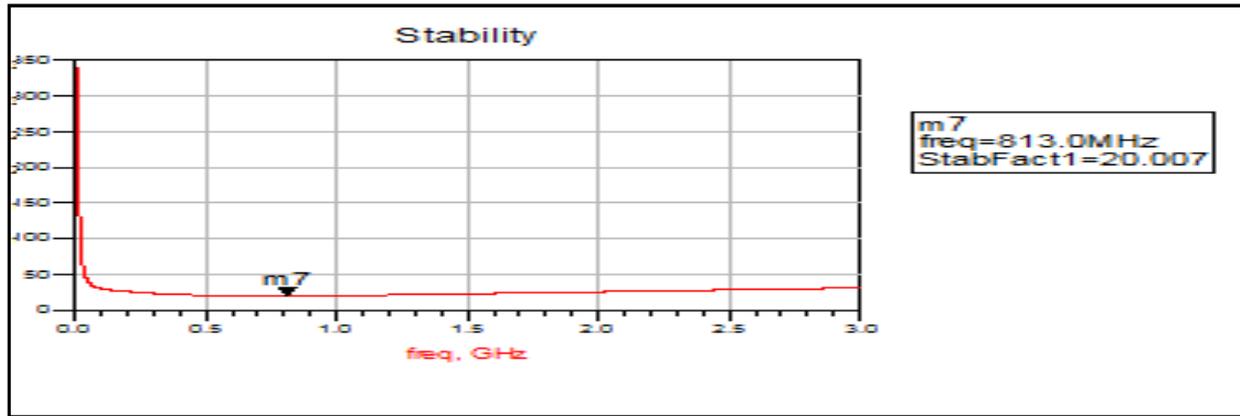


Fig. 8. Stability of the system

Fig. 8. Shows stability of the system over the operating frequency range. For a VGA to be unconditionally stable, the stability factor has to be greater than 1, and β has to be greater than 0. The simulations show that the VGA is stable for its complete operating frequency range.

Table .2. Performance Comparison Of low noise VGA

Ref.	Technology	Gain Range	Noise Figure	Year
[1]	0.18 um CMOS	-20 to 41 db	14db	2011
[2]	0.6 um CMOS	0 to 30db	NA	1995
[9]	0.18 um CMOS	23 to 24 db	6.3 to 7.2 db	2010
[6]	0.9 um CMOS	-10 to 50 db	17 to 30 db	2012
This Work	0.13 um CMOS	-0.81 db to 29.08 db at 40 MHz -3.14 db to 26.644db at 950 MHz	1.747 db to 4.032 db at 40 MHz 1.411 db to 4.995 db at 950 MHz	2015

5 CONCLUSION

In this paper, a low noise variable gain amplifier (VGA) has been designed. In this proposed design a number of attenuators are used, after two stages of amplifier. The proposed VGA was designed using TSMC 0.13 um CMOS technology. This design is proposed to work at frequency range of 40 to 950 MHz. Each attenuator is used for variation in gain. Experimental results shows that, this proposed VGA can cover a wide gain range from -0.81 db to 29.08 db at 40 MHz and -3.14 db to 26.644 db at 950 MHz and the noise figure of proposed designed of VGA ranges from 1.747 db to 4.032 db and from 1.411 db to 4.995 db over the operating frequency range. The results achieved are simulated results obtained on Agilent’s ADS 2009.

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