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Design and Analysis of modified Soft Switching DC-DC Converter with improved voltage regulation for High Frequency applications

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ABSTRACT: In this paper, a modified soft switching DC/DC converter with a full ZVS range with improved output voltage regulation high voltage and high frequency is presented and analyzed. This modified dc-dc converter is designed with two newly proposed half bridge inverter that are situated in parallel among the primary side and phase shifting is made to regulate the output voltage .The novel topology solves the drawbacks of the existing converter .This improved soft switching converter has a major advantage of reduced duty cycle losses and no circulating current. Similarly having reduced output filter. In this proposed converter is provided with proper filter design. The analysis and design is made using mat lab simulation tool.

KEYWORDS: Zero Voltage witching (ZVS), Zero Current Switching, Center Tap Type Rectifier, Phase Shifted PWM Converter.

1 INTRODUCTION

In this paper, the basic soft switching DC/DC converter topology is first presented. This is followed by the modeling of the converter topology, leading to the derivation of a family of converters with improvement and simplification for better functionality and practicality. The resulting family of converters inherits the important advantage of having a reduction in the switch voltage stress. The idea of having soft switching in full bridge DC/DC converter can be traced back in the early years. These soft switching circuits are especially suitable for high power applications (e.g., more than1kw output) because of its high efficiency. In these power levels, the expense of four controlled switches is acceptable. In this system the addition of a small commutating inductor and two low-current clamp diodes essentially eliminates the dynamic losses and the overshoot and the ringing of the rectifier diodes associated with their charge storage and junction capacitance. G. Hua, F. C. Lee, and M. M. Jovanovi´c et al reported an improved full bridge zero voltage switched PWM converter using a saturable inductor core in 1993. The paper discussed about how the saturable inductor which is employed in the full bridge (FB) zero-voltage-switched (ZVS) pulse width -modulated (PWM) converter to enhance its performance. In this proposed system the current and voltage stresses of the switches as well as parasitic oscillations are significantly reduced in this converter topology. The Saturated reactor helps to achieve a wide ZVS range and to reduce circulating current because circulating current increases the losses of the converter. The incorporation of a saturable inductor to the FB-ZVS-PWM converter, a particular member of the ZVS-PWM converters, can minimize all the above drawbacks like achieving wide ZVS range and to reduce circulating current and

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reduces switching losses and also reducing the voltage stress resulting in improvement in the converter performance. The energy stored in a linear inductor is proportional to the square of the inductor current.

Thus the circulating energy in a FB-ZVS-PWM converter is proportional to the square of the load current. For instance, if the converter is designed to achieve ZVS above 20% load, the circulating energy at full load will be 25 times as that needed for discharging the FET capacitances (achieving ZVS for FET's).The situation is somewhat different when the linear resonant inductor is replaced by a saturable inductor. Until now, several soft-switching DC/DC converters have been proposed for the operation of high frequency application. Although the design of these converters has been presented at the operational level for some essential concern such as topologies, analyses, and control have not been thoroughly studied. In this paper, the basic soft switching DC/DC converter topology is first analyzed. This is followed by the modeling of the converter topology, leading to the derivation of a family of converters with improvement and simplification for better functionality and practicality. The resulting family of converters inherits the important advantage of having a reduction in the switch voltage stress.

2 EXISTING CONVERTER TOPOLOGY

The traditional phase-shift full-bridge (PSFB) converter exhibits benefits in medium-to-high-power applications. All primary switches of the converter are turned ON under zero-voltage switching (ZVS) without the help of any auxiliary circuits. The switches' voltage stress is clamped to that of the input voltage. Hence, here high-frequency MOSFETs are suitable as main switches for the converter, which can raise the power density of the converter. However, such a converter has several serious problems: first, the ZVS range of lagging-leg switches is very narrow under the variation of load. For this reason, its conversion efficiency is severely degraded as the load decreases. If the converter is fit for a relatively wide input voltage range due to the design considerations such as the hold-up time requirement, the steady-state duty cycle becomes small and the freewheeling interval lengthens in normal operating conditions. Then, due to this an excessive circulating current appears on the primary side during the freewheeling interval, increasing the primary-side conduction loss and also the turn-off switching loss of the lagging-lag switches. In addition to the small duty cycle has detrimental effects on performance of the converter, such as a large ripple current through the output Inductor *LO*. Especially, in high output voltage applications, a very large inductor *LO* is required to reduce the large ripple current, which results in low power density and increased cost.

In order to overcome the above mentioned problems of the traditional PSFB converter, many studies have been conducted. First, to remove the circulating current and reduce the large output inductor, the frequency-modulated FB converter was presented earlier. The operating range of its switching frequency, however there is change in a wide input voltage range, which leads to difficult in the design, similarly the magnetic components and capacitors also. In this the converter cannot fulfill ZVS in a wide range of load variations. In this proposed system the ZVS range of lagging-leg switches in the traditional PSFB converter can be extended by designing the leakage inductance of the transformer very large or adding an external resonant inductor component with large inductance. However, these approaches will increases duty-cycle loss, which results in high secondary-voltage stress similarly primary-conduction losses also. Another approach is to reduce the magnetizing inductance of the transformer to achieve a wide ZVS range. However, this significantly increases the RMS current stress and conduction losses on the primary side, because of the additional current developed by the magnetizing inductor circulates through all the switches of the converter and transformer at its peak range. In addition, still it has the drawback of a large output inductor in high-output voltage applications. The PSFB converter in the paper uses a saturable reactor on the primary side to achieve a wide ZVS range and to reduce the circulating current. However, too much heat is developed on the saturable reactor core, thus it becomes bulky.

The motive of this paper is to eliminate all the problems of the above mentioned in the existing models which include narrow zero-voltage-switching (ZVS) range, large circulating current, large duty-cycle loss and to design a low output filter for high voltage applications. Similarly to enhance the output voltage and also to reduce switching losses. To reduce the voltage stress is also an important factor.

3 PROPOSED CONVERTER TOPOLOGY

3.1 PHASE SHIFTED PULSEWIDTH MODULATION CONVERTER

The phase shifted pulse width modulation converter is proposed to solve the demerits of the existing converters. This converter provides a soft switching technique along with a full ZVS range and reduced output filter for high voltage and high frequency applications. Some of the major drawbacks that were present in the existing converters are problems related to

duty-cycle loss, full ZVS range, no circulating current, voltage stress and large output filter in high voltage applications. The proposed converter circuit diagram is shown in Fig.3.1.1. The proposed converter is made of two symmetric half-bridge inverters (TSHBIs), with leading-leg and lagging-leg SHBIs, which are located in parallel on the primary side and are driven in a phase-shifting manner to regulate the output voltage of the converter. At the rectifier stage, two full bridge rectifiers sharing two lower-current-rating diodes compared with the main rectifier diodes are employed, because a full-bridge rectifier features low voltage stress in high-voltage applications. The turn's ratio *n* of the proposed converter can be lower than that of the existing converter at the same operating range of duty cycle, which will contribute to the improvement in power loss. The primary RMS current stress in the lagging-leg SHBI in spite of using a small magnetizing inductance of *T*1 is much lower than that of the existing converter design with a small magnetizing inductance, because the average value of the magnetizing current of *T*1 is zero within a half-switching period, and its contribution to the total RMS current at large loads is negligible. Also, it is much lower compared to the existing converter because has a large magnetizing inductance due to the lower turn's ratio. Consequently, in spite of using a small magnetizing inductance of *T*1, the primary conduction losses in the proposed converter become lower than that of the conventional PSFB converter. The ZVS range in the proposed converter is extended using only the magnetizing inductance of the transformer in lagging-leg SHBI, while minimizing the additional conduction loss. In this proposed converter topology, all primary voltages of the transformers are in phase with the primary currents, thus, there is no circulating current. In addition, the area of the reverse current of leading-leg switches as well as its current stress is much smaller than that in the conventional converter, which results in the improvement in the conduction period and turn-off switching losses.

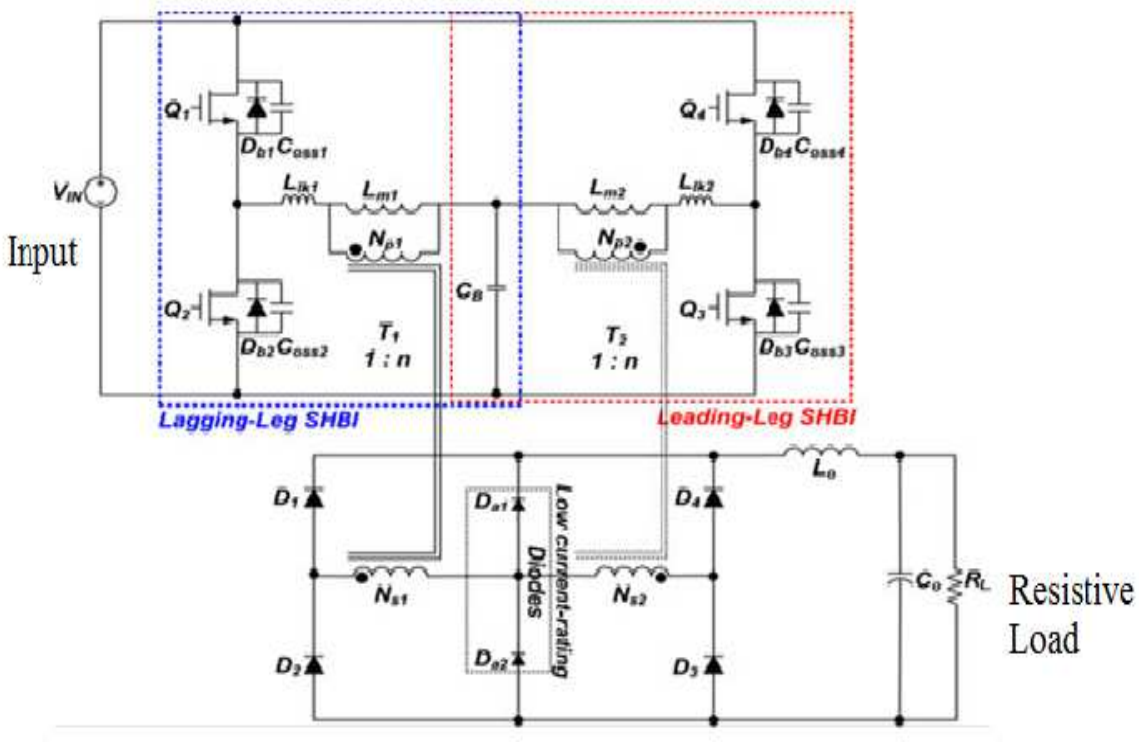


Fig. 3.1.1 Circuit diagram of the modified phase-shifted pulse width modulation converter

The proposed converter system has the following advantages:

- In this system all the switches is turned ON with ZVS under complete load conditions without any additional large resonant inductors or other related circuits, such that the conduction loss caused by the assistant current source extending the ZVS range is minimized due to its reduced conduction path.
- The circulating current in the traditional PSFB converter does not appear in the proposed converter, which contributes to the improvement in the conduction loss.
- The proposed converter has no problems related to an increase of duty-cycle loss. In addition, the conversion ratio is higher than that of existing PSFB converters. These allow that the turn's ratio of the transformers is

designed to be better than that of the counterparts. Thus, the voltage stress across the diode rectifier and the load current reflected to the primary side can be reduced, which leads to the improvement in the conduction loss.

- There is always an input voltage source in the waveform seen by the output *LC* filter. Thus, the value of output inductor is significantly reduced.
- A low profile design becomes a possibility due to the use of two small-sized transformers with low height instead of a large-sized transformer with high height. This results in a slim power supply.

3.2 OPERATING PRINCIPLE OF PROPOSED CONVERTER

The operation principle of the proposed converter in the steady state is studied by using the current and voltage notations and the key operating waveforms of the proposed converter. In this converter all the switches are driven with a constant duty ratio (D = 0.5), ignoring the dead time T dead. The driving signals of the switches in the leading-leg SHBI lead that of the switches in the lagging-leg SHBI. Here, we call the switches in the leading-leg or lagging-leg SHBIs leading-leg or lagging-leg switches, respectively. TSHBIs are operated by adjusting the phase shifted time $T\Phi$ to regulate the output voltage. Each switching period is divided into two half cycles, $t0$–$t8$ and $t8$–$t16$. The circuit showing the current and voltage identifications of the proposed system.

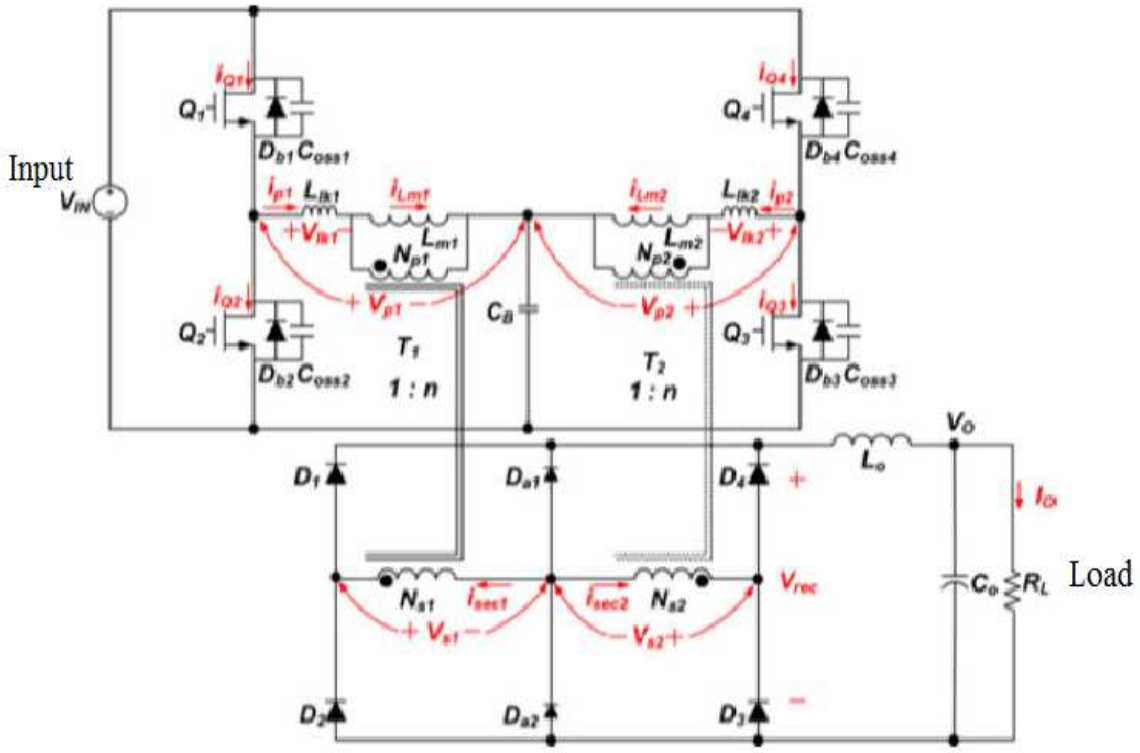


Fig. 3.2.1 Current and voltage indications in the proposed converter

Fig: 3.2.1 shows the current and voltage notations of the proposed converter in the steady state operating condition. The voltage and current flowing through the circuit are indicated using red color indication. The key operating waveforms are also required for the operation of the proposed converter i.e. the voltage and current waveforms across the various components in the proposed phase-shifted pulse width modulation converter. The switching period of the converter is divided into two half cycles, $t0$–$t8$ and $t8$–$t16$. Each half cycle can be subdivided into eight modes of operation.

4 THEORETICAL ANALYSIS AND OUTPUT RESULTS FOR PROPOSED CONVERTER

The performance of the proposed converter is confirmed by the experimental results of a prototype converter realized with the specification of an 80-in plasma display panel (PDP) sustain power module (320–385 V_{dc} input),(205 V_{dc}/5 A output). The prototype converter has to build to check the relevant analysis result which includes

- Input-to-Output Relationship
- Duty-Cycle Loss
- Circulating Current
- Filter Requirement
- Center-Tap-Type Rectifier for Low Voltage Applications

4.1 INPUT TO OUTPUT RELATIONSHIP

Since the durations of modes 2,6 and 8 are very narrow in the proposed converter and hence they can be neglected, then, the rectifier output voltage can be shown as in Figure. Averaging the voltage waveform *V* rec(*t*) in Figure give the dc conversion ratio of the proposed converter as follows:

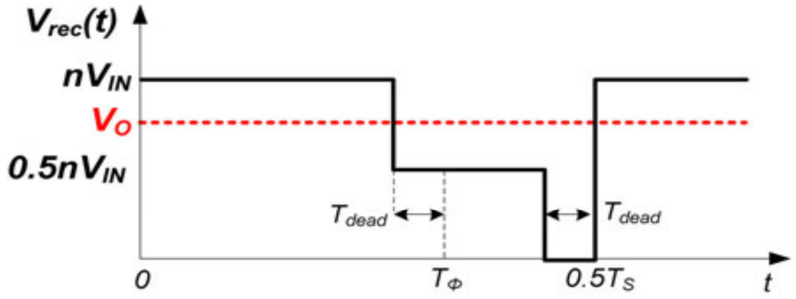


Fig. 5.1.1 Simplified design rectifier output waveform in the proposed converter

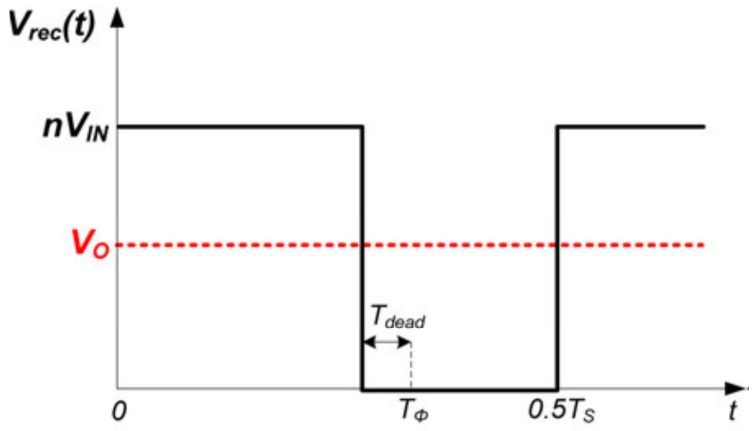


Fig. 5.1.2 Simplified design rectifier output in the existing converter with small leakage (or resonant) inductor

From the figure 5.1.1, it is noted that the gain of the proposed converter is higher than that of the traditional PSFB converter. Therefore, the turn's ratio *n* of the proposed converter can be lower than that of the traditional PSFB converter at the same operating duty cycle, which will contribute to the improvement in power loss.

4.2 DUTY-CYCLE LOSS

In general, it is widely known that utilizing large resonant inductor for extending ZVS range reduces the effective duty-cycle (or increases the duty-cycle loss). To compensate this, the turn's ratio *n* of the transformer is designed to be higher,

thereby increasing the primary-conduction losses and secondary-voltage stress. However, the ZVS range in the proposed converter is extended using only the magnetizing inductance of the transformer in lagging-leg SHBI, while minimizing the additional conduction loss in the converter system. Thus, the present converter has no problems related to the duty-cycle loss.

4.3 CIRCULATING CURRENT

There is the circulating current in the traditional converter, which flows through the transformer and switches although the primary voltage *V* primary (*t*) of the transformer is zero. This will raise the conduction losses. Similarly in this proposed converter, all primary voltages of the transformers are in phase with the primary currents, thus, there is no circulating current. In addition, the area of the reverse current of leading-leg switches as well as its current stress is much smaller than that in the traditional converter, which impacts in the improvement in the conduction and turn-off switching losses of the converter.

4.4 CENTER-TAP-TYPE RECTIFIER FOR PROPOSED CONVERTER

The rectifier structure is a kind of full-bridge rectifier. In general, two types of rectifiers are widely used, i.e., full-bridge rectifiers and center-tap rectifiers. Although a full bridge rectifier employs four diodes, compared to a center-tap rectifier, it offers benefits when it comes to transformer size and voltage stresses on the diodes for high voltage application. In the case of a center-tap rectifier, only two diodes are employed and there is only one diode in the secondary current path which results in less conduction loss for low voltage applications only.

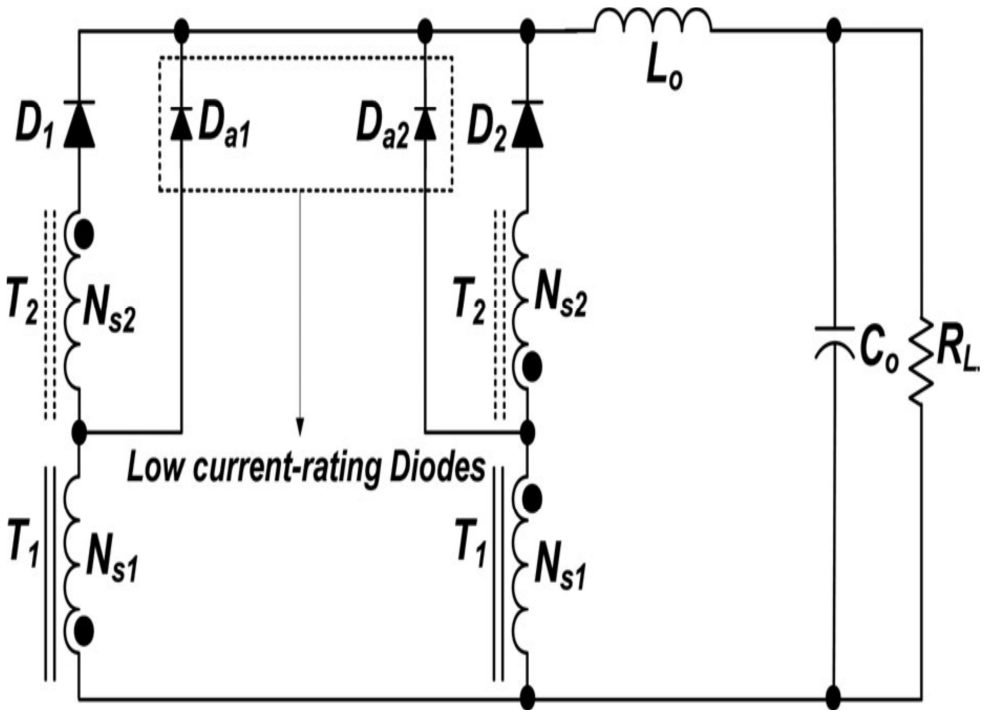


Fig. 5.4.1 Center-tap-type rectifier for the proposed converter design.

A center-tap-type rectifier suitable to the proposed configuration for low voltage applications is presented in the paper. The primary structure is the same and only the secondary structure is changed. Each transformer has two secondary windings and they are connected in series by turns. *D*1 and *D*2 are the main diodes, and *Da*1 and *Da*2 are the auxiliary diodes. The operational principle of the proposed configuration with the center tap rectifier is identical to the full-bridge rectifier.

5 SIMULATION ANALYSIS AND OUTPUT OF THE PROPOSED CONVERTER MODEL

The simulation of the proposed phase-shifted pulse width modulation converter is done using MATLAB to verify the relevant analysis results which include Input to Output relationship, ZVS condition, Duty cycle loss, filter requirements. The performance of the proposed converter is confirmed by the experimental results of a prototype converter realized with the specification of an 80-in plasma display panel (PDP) sustain power module. The basic parts of the proposed phase-shifted pulse width modulation converter consists of two symmetric half-bridge inverters (TSHBIs), leading-leg and lagging-leg SHBIs, which are located in parallel on the primary side of the transformer, two symmetric half-bridge inverters (TSHBIs), leading-leg and lagging-leg SHBIs, which are located in parallel on the primary side of the transformer.

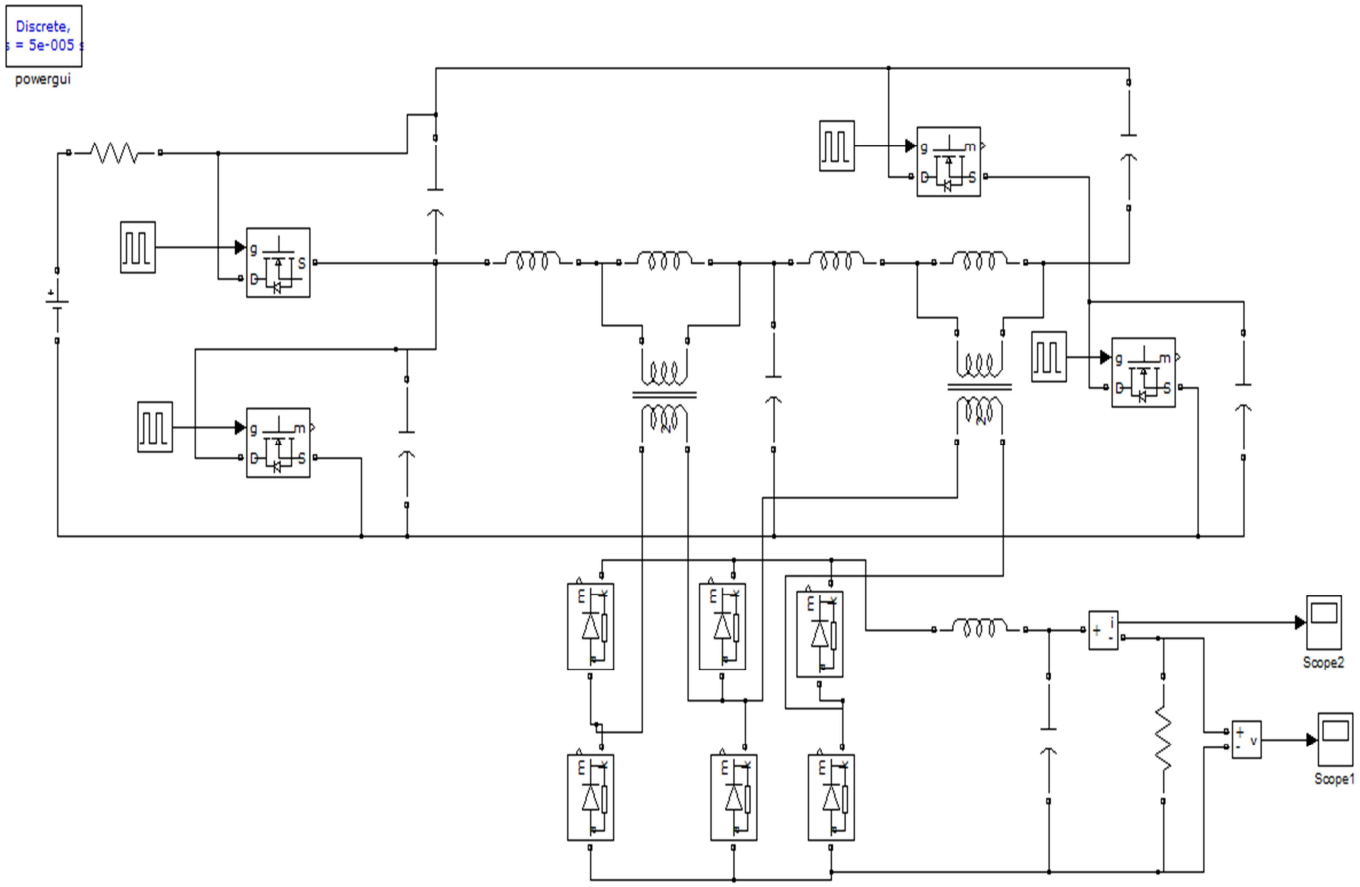
Table 1. Table of components

Main Switches($Q_1 \sim Q_4$)	SPW24N60C3(600V,24A)
Rectifier diodes($D_1 \sim D_4$)	16CTU04(400V,16A)
Auxiliary diodes(D_{a1}, D_{a2})	RURD460(600V,4A)
Main transformers(T_1, T_2)	Core:PQ3535 Turns Ratio:0.667 For T1, For T2, L_m:240µH,L_{lk}:6.08µH L_m:1.2mH, L_{lk}:8.47µH
Blocking capacitor(C_B)	2.2µF/250V
Output inductor(L_o)	125µH, MPP core
Output capacitor(C_o)	47µF/250V

The above given is a table containing the various component list and the specification which is been used for the above circuitry for getting the prototype output voltage and the prototype output current. Using the above specified components in the table the required prototype output can be achieved, the above components are used in the final stage of the DC/DC converter i.e. the rectifier stage for the rectification and filtration of the output. This proposed system is analyzed with nominal input voltage, i.e., 385-420 V and a full load current of 5 A.

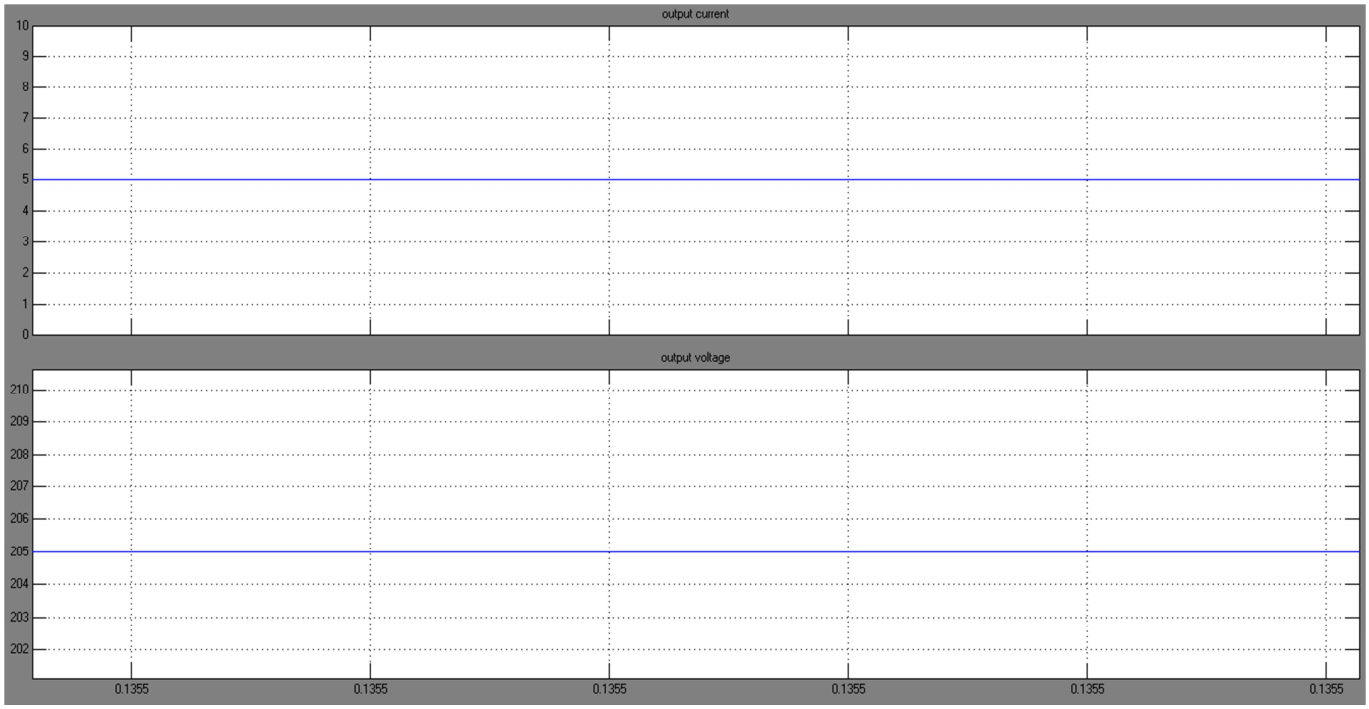
1) Input voltage: (*V*IN = 380–420 V);
2) Output voltage: (*VO* = 205 V);
3) Maximum output current: I_O (max) = 5 A;
4) Switching frequency: f_S = 100 kHz.

The simulation diagram of the proposed modified phase-shifted pulse width modulation converter is done in MATLAB and the prototype output needed for the result analysis is obtained.



Simulation diagram

6 OUTPUT WAVEFORMS



7 CONCLUSION

This paper has presented a modified soft-switching dc/dc converter that can overcome the remedies the of existing PSFB converters, such as narrow zero-voltage-switching (ZVS) range, large circulating current, large duty-cycle loss and a substantial output filter used in high voltage applications. In this presented system, the theoretical analysis has also been provided to show that the proposed converter has the performance over traditional PSFB converters. The regulated output voltage is obtained and also the voltage stress is minimized. Hence the efficiency of this presented converter is increased compared to the conventional converter. The input voltage is obtained as regulated output in this proposed converter.

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