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CMOS LNA Design for Ultra Wide Band - Review

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ABSTRACT: Low Noise Amplifier (LNA) functions important role in receiver designs. In, microwave receiver LNA circuit plays important role in quality factor of receiver. At radio frequency range, trade-off characteristics like gain, noise figure, stability, power consumption and complexity forces designer for various circuit's simulation for optimizing those. An LNA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. For short range and high data rate wireless applications UWB technology offers a promising solution to the radio frequency. As LNA is most important block included in the UWB front-end RF receiver, we focused this paper on review of LNA design using CMOS technique.

KEYWORDS: Low Noise Amplifier (LNA), Ultra Wide Band (UWB), Complementary Metal Oxide Semiconductor (CMOS), Signal to Noise Ratio (SNR),

1 INTRODUCTION

Due to CMOS technology cost effectiveness and compatibility with silicon-based system on-chip (SOC) technology, it can be considered the most prevailing technology for RF integrated circuits (RFIC) implementation. In February 2002, UWB frequency range (3.1 GHz-10.6 GHz) was approved by the Federal Communication Commission (FCC) for commercial application [1]. UWB wireless technology has the capability of transmitting data over a wide spectrum of frequency bands with very low power, high data rates and at very low cost.

LNA can be considered one of the most important blocks included in the UWB front-end RF receiver. The role of the LNA is to receive and amplify signals over the ultra-wide band frequency range. LNA specifications include low and flat noise figure, high and flat power gain, good input and output impedance matching, good reverse isolation and acceptable linearity.

The UWB technology offers several advantages, such as wide bandwidth, large throughput, and robustness to jamming. This technology is suitable for short range and high data rate wireless applications. UWB technology offers a promising solution to the radio frequency (RF) spectrum drought by allowing new services to coexist with the other radio systems with minimal or no interference. An UWB CMOS LNA design using an input CG stage can be used to reduce the circuit complexity and power consumption.

This paper reviews various low Noise Amplifier Parameters and LNA design circuits using Current reuse circuit and CMOS Circuit using shunt- series Cascode stage.

2 UWB TECHNOLOGY

Ultra Wide Band (UWB) technology has been designed to bring convenience and mobility of high speed wireless communication to homes and offices. It is specifically designed for short range Wireless Personal Area Networks (WPANs). In the spring of 2002, the Federal Communications Commission (FCC) established an unlicensed communication band (3.1-10.6 GHz) and restricted transmitted power levels within that band to be below the noise floor, specifically below-41.3dBm/MHz, thereby allowing for the possibility of commercial Ultra-Wideband (UWB) systems.

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There are basically two different system level communication strategies employed to efficiently utilize the entire UWB spectrum, namely, direct sequence UWB (DS-UWB) and carrier-based orthogonal frequency division multiplexing (OFDM) [6]. The Multi-band OFDM Alliance (MBOA) supports a type of OFDM architecture referred to as MBOFDM. The UWB-Forum is proposing a form of IRUWB called Direct-Sequence UWB (DS-UWB).

2.1 UWB TRANSCEIVER

A basic block diagram of the UWB transceiver, including a transmitter and a receiver, is shown in Figure 2.1. The baseband Digital Signal Processing (DSP) unit controls the messaging and signaling of information. The DSP unit also synchronizes the system clock. The main function of the receiver is to amplify the signal without amplifying the noise.

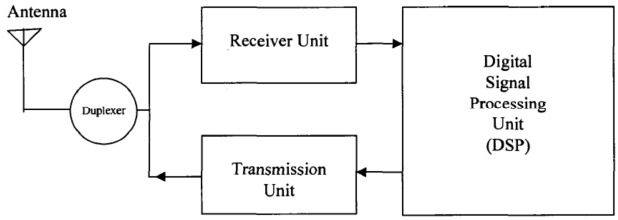

Figure 2.1:Block Diagram of UWB Tranreceiver

The block diagram of a UWB receiver is shown in Figure 2.5. The receiver features a Low Noise Amplifier (LNA) followed by a mixer (demodulator). The mixer removes the carrier from the received radio frequency signal. Usually there is an automatic gain control block between the mixer and the Analog to Digital Converter (ADC). The purpose of this block is to balance the amplification or attenuation of the received signal in a way that it utilizes the maximum range of the ADC. The analog to digital converter then converts the analog signals to digital data which is fed to the DSP to process the transmitted data. The signal is then fed to the DSP block for baseband processing. In this context it is clear that an ultra-wideband LNA should pass all the frequencies between 3.1 to 10.6 GHz. Such an amplifier must feature wideband input matching to a 50 Q antenna for noise optimization and filtering of the out-of-band interferers. Moreover, it must show flat gain with good linearity and minimum possible noise figure over the entire bandwidth.

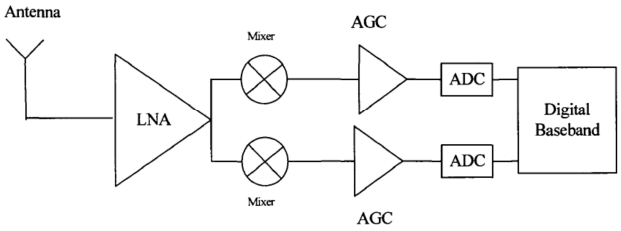

Figure 2.2: Block diagram of receiver

3 LNA PARAMETERS

The Low Noise Amplifier (LNA) is the first gain stage of a receiver. It must meet several specifications at the same time, which makes its design challenging. The received signal should have a certain Signal to Noise Ratio (SNR) in order to allow proper detection. Therefore, noise added by the circuit should be reduced as much as possible. The gain, stability and noise figure of the LNA are usually measured using the scattering parameters (S-parameters)

3.1 TWO-PORT S-PARAMETERS

Scattering Parameters (sometimes called S-parameters) have become the default standard in characterizing the performance of microwave systems and circuits. S-parameters relate incident and reflective waveform amplitude and phases between every port within a two-port network by,

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \quad (3.1)$$

Where, -*Vi* = voltage phasor of the waveform traveling away from port-*i* (reflected waveform), and *Vi* = voltage phasor of the waveform traveling toward port-*i.*

Fig3.1 gives a graphical depiction of the traveling reflective and incident waveforms acting on a two port network.

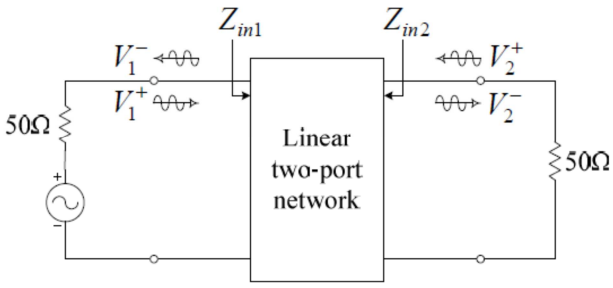

Figure 3.1: Two-port network

3.2 IMPEDANCE MATCHING

In order to reduce reflections, input and output matching networks must be added to the analog signal processing device. In addition to maximizing the power transferred (no waveform reflections) to the load, matching networks can also be used to minimize noise influence and/or to linearize the frequency response of a system. For DC circuits, the maximum power theorem states that the maximum power available from the source will be transferred to the load provided the real internal source resistance is equal to the real impedance of the load.

For AC Circuits, the maximum power transfer occurs when the complex internal impedance of the source equals the complex conjugate of the load impedance. Therefore, when the source is connected to the load, the internal impedance of the source connects in series with the load impedance and the inductive and capacitive reactance of the load and source compensate for each other and a real impedance results. Since the imaginary part of complex impedance depends on frequency, complex impedance matching is very difficult to realize over a very large bandwidth. Circuits such as an LNA will load the source with a very complex impedance profile versus frequency, and thus a simple complex conjugate is hard to realize over all of the frequency. Wideband impedance matching can be realized with either high order passive networks or active devices

3.3 NOISE FIGURE

Noise figure has commonly been adopted as the metric of choice when characterizing receiver sensitivity. Noise factor (F) is measured as the ratio of input signal to noise ratio and degraded signal to noise ratio.

$$F = \frac{\left(\frac{S}{N}\right)}{\left(\frac{S}{N}\right)_{out}} \quad (3.6)$$

Noise figure is essentially the same metric of performance except expressed in a more convenient manner and is given by following equation, which is simply the logarithmic to base ten of noise factor [7].

$$NF = 10\log(F) \quad (3.7)$$

3.4 STABILITY

Stability may be the most important property of any system. If the system is not stable, then it may be prone to uncontrollable oscillations which can internally damage the system. And depending on the system application, it could be hazardous to system operators. In the case of an LNA however, un-stability can cause internal circuitry damage and ensure that the amplifier will not work. The Rollett stability factor, denoted by k, is given by the following expression,

$$K = \frac{1 \quad |S_{11}|^2 \quad |S_{22}|^2 + |\ \ |^2}{2|S_{12}\|S_{21}|} \tag{3.8}$$

Where, $\Delta = S_{11}S_{22} - S_{12}S_{21}$

An amplifier is unconditionally stable if $K > 1$

4 CMOS LNA CIRCUITS

4.1 CMOS USING CURRENT REUSE CIRCUIT

Figure 4.1 shows the CMOS UWB LNA utilizing the current-reused technique.

LC high-pass filter of C1 and L1is employed as the input matching network, and the inter-stage network composed of the inductors LG, LD and capacitor CG performs a current-reused function to achieve high power gain. In addition, an inductor LB is connected between the main circuit and the output buffer for further bandwidth extension due to a series LC resonance with the gate capacitance of M4 [7].

The current-reused configuration can be considered as a two stage cascade amplifier, where the first stage is the CS amplifier (M_1), and the second stage is the cascode amplifier (M_2 andM_3) with an additional buffer stage at the output. NotethatM$_3$ is the common-gate stage of the cascode configuration, which eliminates Miller effect and provides a better isolation from the output return signal. The purpose of using L_G and C_G is to perform a series-resonant with C_{gs} of M_2 for a low impedance path, while the impedance of L_D is adequately large in the desired bandwidth to provide a high impedance path to block the signal [2].

Current-reused function can work properly as L_D exceeds a certain value, and is not affected by the selection of C_G and L_G. The resonate circuit composed of L_G and C_G .Therefore, the current- reused function is maximized at around the resonant frequency [3].

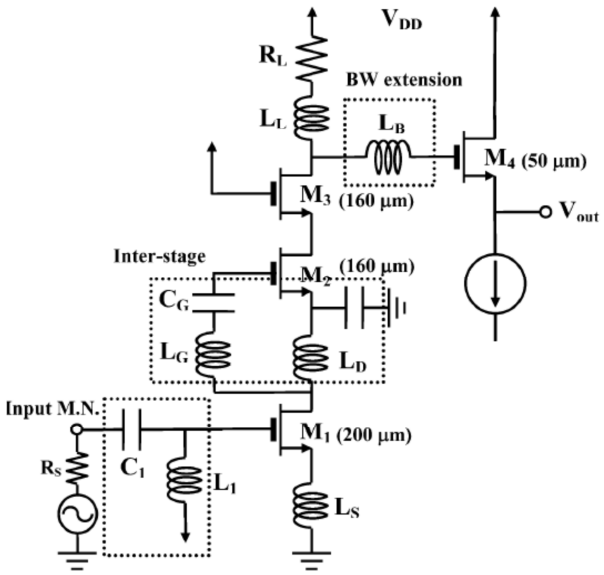

Figure 4.1: Current Reused LNA

4.2 CMOS USING SHUNT- SERIES CASCODE STAGE

Low Noise Amplifier shown in Fig 4.1consists of three stages- input stage, cascode stage, and output stage.

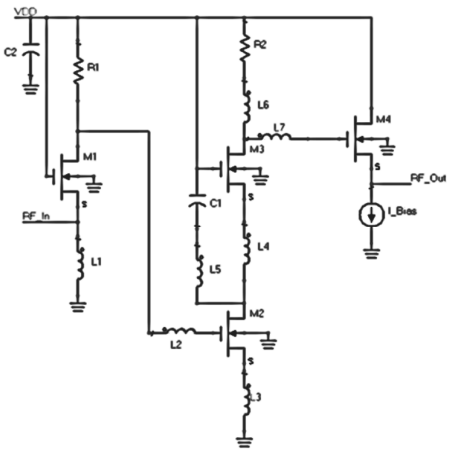

Figure 4.2: LNA Design

4.2.1 INPUT STAGE

The input stage for above LNA has a CG amplifier as the first stage to provide input matching. In CG amplifier the resistance looking into the source terminal is 1/gm.

The input impedance is given by the equation,

$$Z \approx \frac{sL_1}{1+\left(sC_{gs1}+g_{m1}\right)sL_1} \tag{4.1}$$

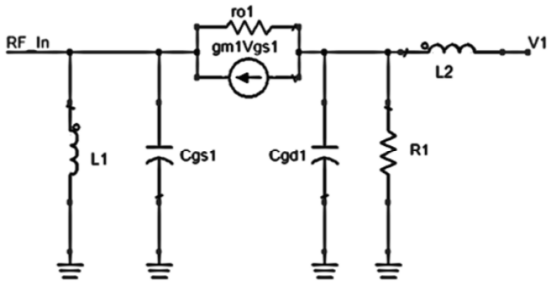

Figure 4.3: Equivalent Circuit for Input Stage

A conventional Cascode Amplifier employing current reuse technique and shunt-series peaking is used as the second stage in order to provide a sufficient gain with a wider 3-dB bandwidth [4]. The current reuse [3] topology is constructed by using C1, L4 and L5. The combination ofL5 and C1 provides a low resistance path, as a consequence of which the input signal can be amplified twice through the two paths available. The shunt-series peaking [5] is used to enhance the bandwidth

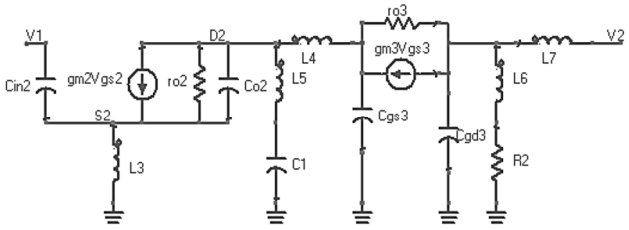

Figure 4.4: Equivalent Circuit for Cascade Stage

The gain achieved by this second stage is given by the equation,

$$A_{v2} = \frac{g_{m2} g_{m3} Z_{L2} Z_{L3}}{1 + g_{m2}(sL_3)} \tag{4.2}$$

Where,

$$Z_{L2} \approx \left(sL_5 + \frac{1}{sC_1} \right) // \left(sL_4 + \frac{1}{sC_{gs3}} + \frac{1}{g_{m3}} \right) \tag{4.3}$$

$$Z_{L3} \approx (sL_6 + R_2) // \left(sL_7 + \frac{1}{sC_{gs4}} + \frac{1}{g_{m4}} \right) \tag{4.4}$$

4.2.2 OUTPUT STAGE

A buffer is added to provide the output impedance matching. The equivalent circuit for output stage is shown in fig 4.4. This buffer is simply a source follower (M4) which has low output impedance thereby enabling easy output matching. The drain resistance of the transistor M4 serves as the load of the UWB LNA.

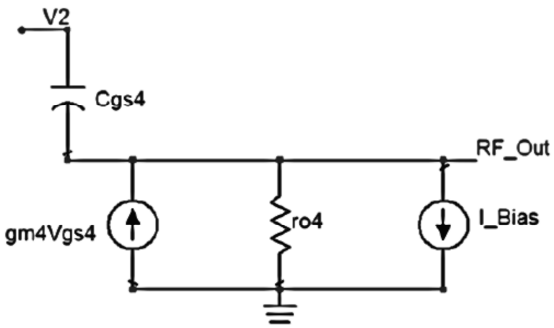

Figure 4.5: Equivalent Circuit for Output Stage

The output impedance of the proposed LNA is given by the equation,

$$Z_{out} \approx r_{o4} \tag{4.5}$$

The gain of buffer is given by equation,

$$A_{v3} \approx \frac{g_{m4} r_{o4}}{1 + g_{m4} r_{o4}} \tag{4.6}$$

So, overall gain of proposed LNA is given by equation,

$$A_{v,total} = A_{v1} \times A_{v2} \times A_{v3} \tag{4.7}$$

5 CONCLUSION

In LNA design it is required to achieve a high power gain in order to reduce the effect of noise introduced by the subsequent stages at the receiver front end, high noise factor to have original signal and also input matching, output matching, reverse isolation, power consumption, stability are taken into consideration. In order to improve gain of LNA CMOS current reused technology is used. If bandwidth enhancement is required CMOS using shunt series cascode stage is used.

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