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Comparative Analysis of 64-bit Low Power SRAM Cell Designs by Using Charge Recycling Scheme

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ABSTRACT: SRAM cell design takes a big fraction of the entire power and die area in high performance processors. The overall power consumption in SRAM can be reduced either by decreasing the dynamic or static power. A Charge Recycling (CR) is a very efficient means to reduce the power dissipation in the write cycle of SRAM cell designs. To keep this point in view, this paper represents the simulation of four 64-bit SRAM cell topologies by using Charge Recycling scheme and their comparative analysis on the basis of their average write power consumption. The 64-bit SRAM cell designs are arranged in 8X8 form. Simulation reveals that 64-bit 9T SRAM cell with CR perform better than others in the term of power consumption but if die area and average power consumption both considers, then 64-bit 7T SRAM cell with CR perform well as compared to 64-bit 9T SRAM cell with CR. All the simulations of SRAM cell designs have been carried out on 180nm, 130nm and 100nm CMOS technology at 100 MHz and Vdd = 1.8 V.

KEYWORDS: low power SRAM, power consumption, CR, charge recycling scheme, write cycle, 6T, 7T, 8T, 9T.

1 INTRODUCTION

Demand of today's electronic market is to have high performance, high speed and long battery life devices become a major concern for VLSI on chip designs. To achieve this, SRAM plays a vital role which is used such as a cache memory in high speed applications. As cache memory presents very close or in the processors, the power dissipation in the form of heat in SRAM may create a problem for the processor. Hence a low power SRAM cell design is needed. SRAM tends to have a large number of bits per word, as system become more complex [1]. In this type of SRAM, the power dissipation occurs in the form of dynamic power and static power [3]. These are the two major sources of power dissipation in digital CMOS circuits, each one being affected by different factors and influencing the system in a different way.

Static power dissipation occurs by the leakage currents and sub-threshold currents. The power dissipation is usually quite small in the reverse biased p-n junction which is accountable for the leakage currents but sub-threshold conduction exponentially depends on parametric conditions so therefore it is important, to be considered in some circumstances. Dynamic power dissipation occurs mainly due to the power consumed during read and write operation or in other words, charging and discharging of the load capacitance during circuit switching and due to short circuit power consumption. A dynamic power account for the majority of the total power in digital CMOS VLSI circuits is dissipated during the rise time and fall time of the highly capacitive data bit lines [2]. Dynamic power dissipation is more during write cycle than that of the static power dissipation in low power SRAM cell due to the full voltage swing in bit lines.

Many authors proposed different approaches to reduce power consumption in SRAM but reusing of a charge on the adjacent bit line which was already used charge on a bit line to create a low voltage swing for the operation of writing, is a very efficient mean to reduce the power dissipation. This technique was introduced by H.Yamauchi et al. [4] in bus architecture for ultrahigh data rate low power on chip design. B. D. Yang and L. S. Kim were proposed charge recycling scheme on ROM architecture [5] then by using hierarchical bit line architecture and local sense amplifier SRAM cell was proposed [6]. But K. Kim

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et al. were the first to proposed charge recycling scheme directly to bit lines to reduce dynamic power consumption during the operation of writing, associated with the voltage swing created on bit lines [1]. B. D. Yang then again used this scheme for the both read and write operation [2]. A zero aware asymmetric cell was proposed to minimize power consumed to write '0' only and three bit lines in each column increase total capacitance for the memory [7]. A shared bit line architecture was proposed by H. Morirnura et al. [8] in which dynamic power reduces but no one can perform read and write operation in a row on adjacent cells.

After carefully analyzing all the previous work this paper proposed a comparative analysis of 64 bit low power SRAM cell designs using already used charge on the adjacent bit line during write cycle on the basis of their average power consumption.

This paper is arranged in the following manner in VI sections. Section II briefly describes schematic of 6T, 7T, 8T and 9T SRAM cell designs. In section III, charge recycling scheme is explained with the help of detailed circuit diagram and operational waveform. Section IV describes schematic of 64-bit low power CMOS SRAM cell designs by using charge recycling scheme and section V shows the results on the basis of their average power consumption during write cycle. All discussions are summarized in section VI and at the end references are given.

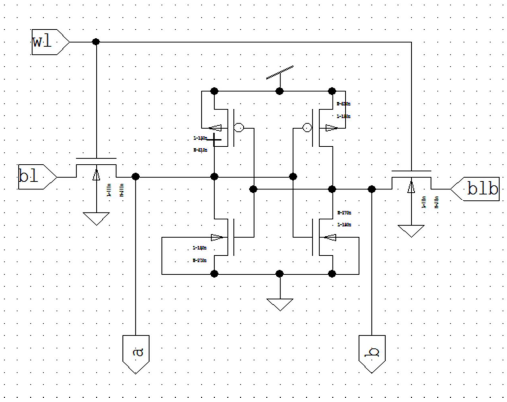

Figure 1. Schematic of 6T SRAM cell

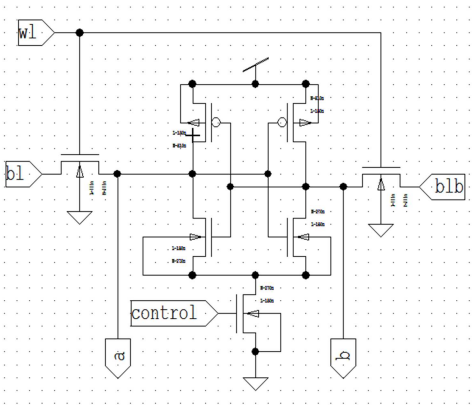

Figure 2. Schematic of 7T SRAM cell

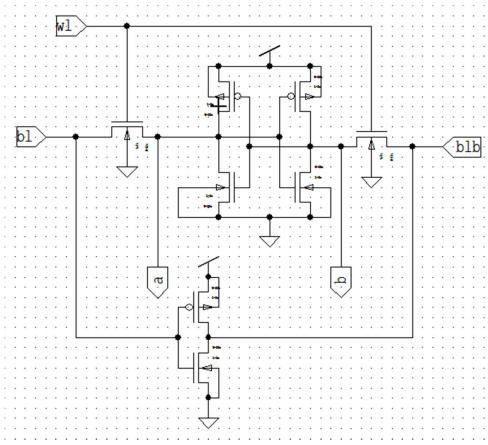

Figure 3. Schematic of 8T SRAM cell

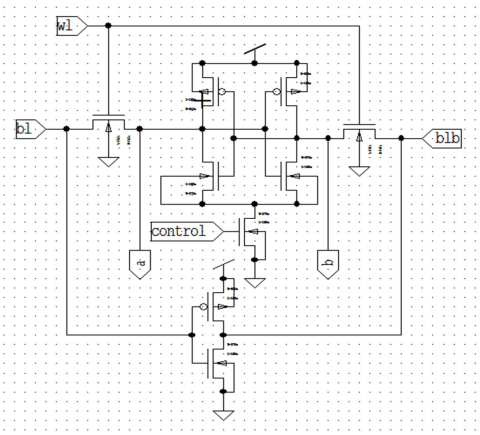

Figure 4. Schematic of 9T SRAM cell

2 SCHEMATIC OF LOW POWER SRAM CELL DESIGNS

A 6T SRAM cell consists of two cross connected inverter with two transistors of access as shown in figure 1. A cell gains access by the word line (WL) that controls two NMOS transistors of access and these transistors controls if the cell must get connected to the bit lines (BL and BLB). For the operation of writing one bit line is to be at high place and another bit line is to be in conditions of fall. In SRAM, the active power is dissipated due to his full swing nature in write cycle [2].

7T SRAM cell consists of an extra N MOS transistor than that of the 6T SRAM cell. An additional N MOS transistor connected to the source of driver N MOS transistors of the SRAM memory cell, enable small swing of bit lines in the write operation and also act as a sense amplifying memory cell which is used to achieve read disturb free operation. It is controlled by a separate control signal as shown in figure 2 [9].

8T SRAM cell is created by adding one more inverter in 6T SRAM cell as shown in the figure 3. An additional inverter helps to reduce power consumption during write cycle. The upper circuit of 8T SRAM cell is essentially a conventional SRAM cell. Data is stored within this circuit. Its working is similar to that of 6T SRAM cell operation.

9T SRAM cell is created by using an additional inverter as used to design 8T SRAM cell with one more NMOS transistor which is connected totally as like in designing of a 7T SRAM cell as shown in figure 4. In other words, 9T SRAM cell is the combination of 7T and 8T SRAM cell which helps to enable a small swing of bit lines and also with the help of additional inverter to reduce more power consumption during write cycle.

3 CHARGE RECYCLING SCHEME

Charge recycling scheme is that in which already used charge on a bit line is reused to produce a low voltage swing on the adjacent bit line throughout write operation. In this scheme,

Two switches on ‘b1’ and ‘b2’ nodes are used as transmission gate switches and these switches are ordered by signal 'in' and 'in1'. Data in the form of ‘bl’ and ‘blb’ are connected with nodes ‘b1’ and ‘b2’ through these two switches. An extra pass transistor switch for charge recycling is connected between both the nodes ‘b1’ and ‘b2’, controlled or ordered by signal 'cr' and 'crb' (Charge Recycle and Charge Recycle bar). Two capacitors C1 and C2 are connected to nodes b1 and b2 at one end and other end is grounded as shown in the figure 5.

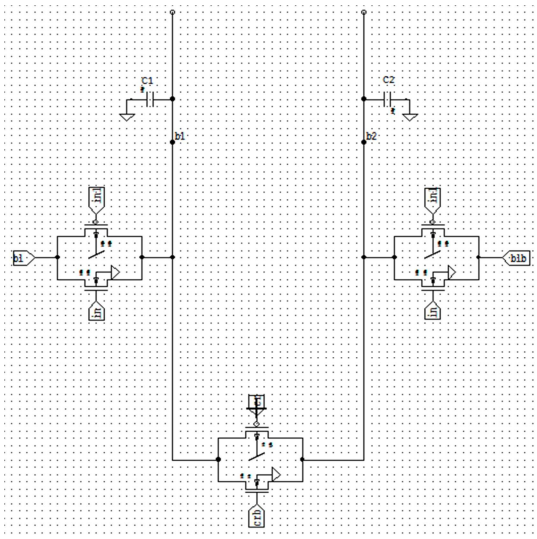

Figure 5. Schematic of a charge recycling scheme [3].

During a first cycle, both the switches on ‘b1’ and ‘b2’ nodes are closed and switch between the nodes is open. Capacitor C1 on a node ‘b1’ is charged to zero volts and C2 on a node ‘b2’ is charged to V volts. Then during a cycle which is introduced as an extra cycle between first and second cycle, switches on ‘b1’ and ‘b2’ nodes are open and switch in between ‘b1’ and ‘b2’ nodes is closed. In this way node ‘b1’ and ‘b2’ shorts so that the charges on capacitors redistributed equally. The levels of voltage on both the capacitors are V/2 volts after redistribution of charges without the necessity of any further electric charge[3].

After this in the next cycle, C1 is charged from V/2 volts to V volts and C2 is discharged from V/2 to zero volts and in the normal case as shown in the figure 6, capacitor C1 is to be fully charged and C2 is to be fully discharged but by using charge recycling scheme, charges on C1 and C2 are charged and discharged from V/2 volts as shown in the figure 7. This scheme saves power consumption as the previously used charge is reused on the adjacent bit line and also increases the speed of SRAM during write operation [1-3].

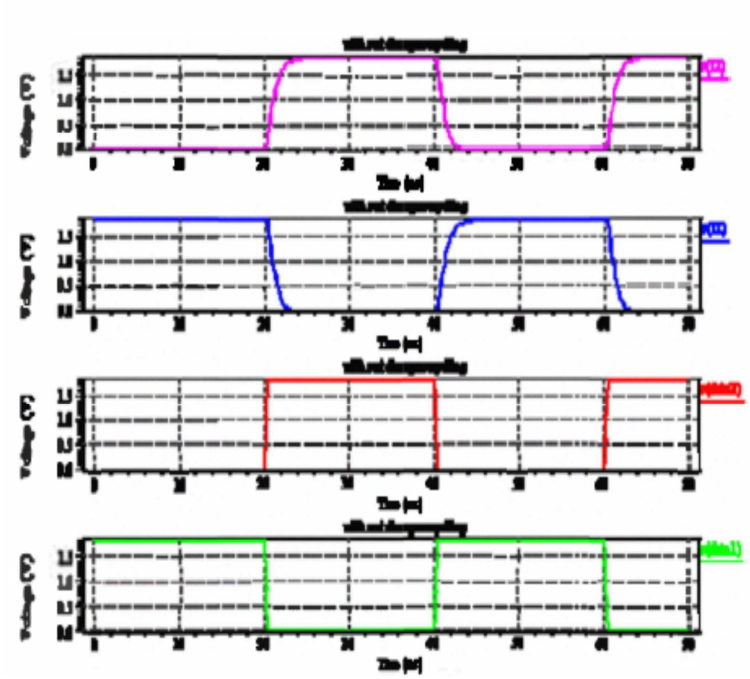

Figure 6. Waveform of a normal operation.

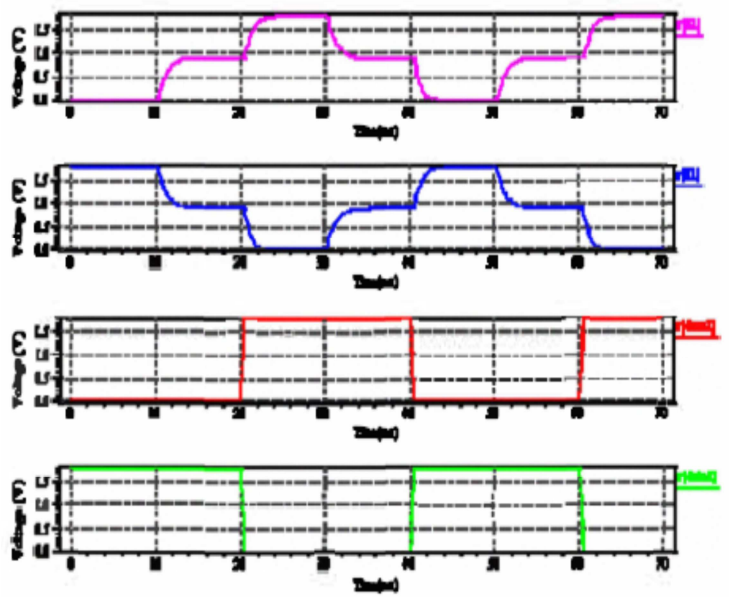

Figure 7. Waveform by using CR.

4 SCHEMATIC OF 64-BIT LOW POWER SRAM CELL DESIGNS BY USING CHARGE RECYCLING SCHEME

The charge recycling scheme is implemented on 64 bit low power SRAM and simulated on 180nm, 130nm and 100nm CMOS technology. Schematic of 64 bit 6T low power SRAM using charge recycling scheme is shown in figure 8, in which SRAM cell design is organized in 8X8 form i.e. 8 rows and 8 columns. Each column has three transmission gates. Two transmission gates are used as switches to separate the data from bit lines and one transmission gate is used as a switch for recycling of a charge of bit lines of every column throughout the charge recycling cycle.

A transmission gate which is used as a switch for recycling of a charge connected in between bl and blb lines. Other two transmission gates are connected to bl and blb lines respectively to separate the data on bl and blb during the charge recycling

scheme. When switches connected to bl and blb are ON and switch in between bl and blb remains OFF then it works as a conventional SRAM.

In the next cycle, switches connected to bl and blb are OFF and switch in between bl and blb is ON. During this period, the previous charges on the bit lines redistributed equally on both the bit lines and voltage level can say, will be Vdd/2 on both the bit lines. After this, one line charges from Vdd/2 to Vdd and other discharges from Vdd/2 to ground but power is also consumed by the switches used for the charge recycling scheme. So this process saves almost half charge is to be supplied from the source. Overall 24 transmission gates are used as switches for charge recycling scheme in 64 bit SRAM. As it saves almost half charge in every cycle, hence the power dissipation reduces at a large amount.

Similarly this scheme works on 7T and 9T low power SRAM cell design as shown in figure 9 and figure 11, in which an additional NMOS transistor provides help to charge recycling scheme by enabling a small swing on bit lines to reduce power consumed during write cycle as discussed earlier whereas in 9T presence of an additional inverter also help to reduce more power consumption similarly like this additional inverter helps in 8T SRAM cell. Figure 10 shows the schematic of 64 bit 8T low power SRAM cell design by using charge recycling scheme.

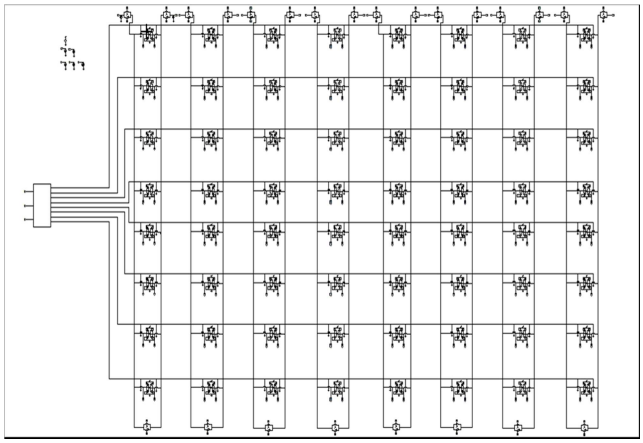

Figure 8. 64-bit 6T low power SRAM cell using CR

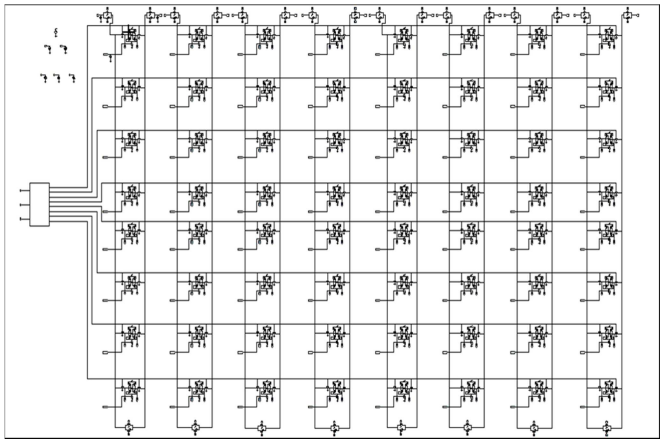

Figure 9. 64-bit 7T low power SRAM cell using CR

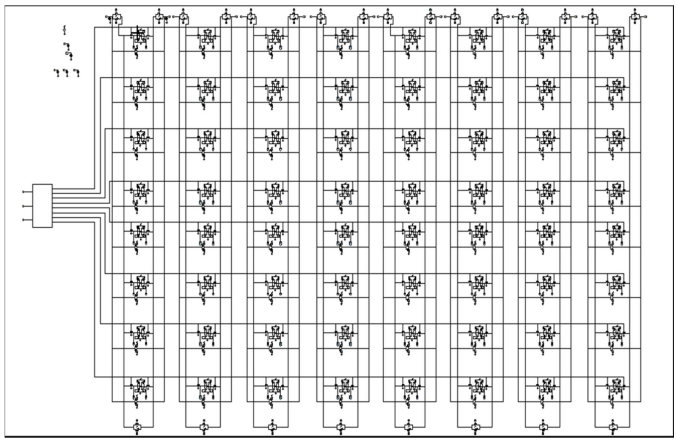

Figure 10. 64-bit 8T low power SRAM cell using CR

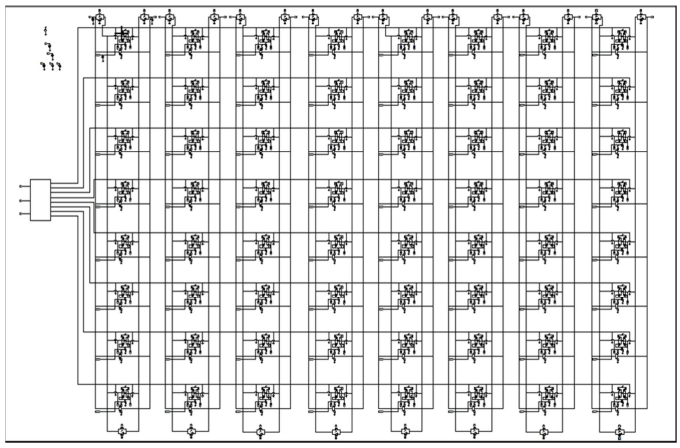

Figure 11. 64-bit 9T low power SRAM cell using CR

5 RESULTS

Table I. shows the comparative analysis of 64-bit low power SRAM cell designs by using charge recycling scheme on the basis of their average power consumption. All the simulations have been carried out on 180nm, 130 nm and 100nm CMOS technology respectively at 100 MHz and Vdd = 1.8V.

64-bit 6T SRAM cell consumes average of 3.060222mW, 2.676775mW and 2.613168mW power, 64-bit 7T SRAM cell consumes average of 1.596712mW, 0.157291mW and 1.621887mW power, 8T SRAM cell consumes average of 2.213734mW, 1.998538mW and 2.013592mW power and 9T SRAM cell consumes average of 1.319183mW, 0.106387mW and 1.229541mW power at 180nm, 130 nm and 100nm CMOS technology respectively. As technology scales down more, the average power consumption increases at Vdd= 1.8V. Average power consumption results are also shown in the form of bar chart in figure 12.

Average power consumption results of 64-bit SRAM cell designs by using CR scheme in this paper is less than as compared to SRAM cell designed by V.K. Singhal [3] and a low power SRAM using charge recycling proposed by K. Kim [1].

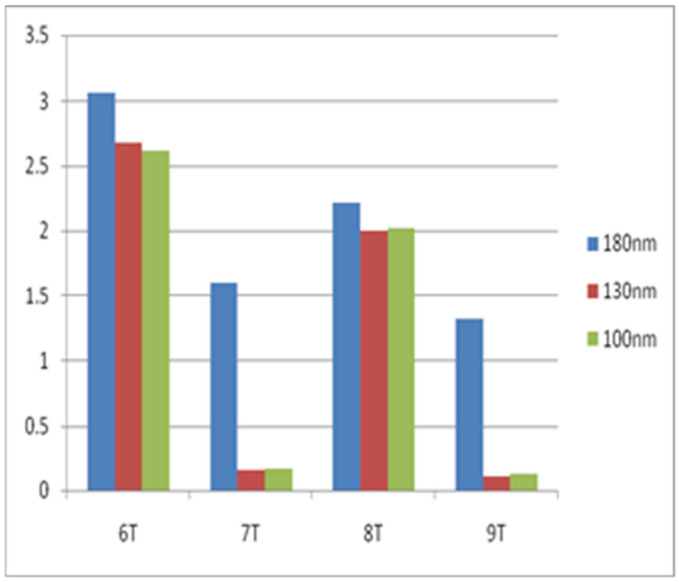

Figure 12. Average power consumption of 64-bit SRAM cell designs using charge recycling scheme.

Table 1. comparison of 64-bit low power SRAM cell designs by using charge recycling scheme on the basis of their power consumption.

Technology	6T SRAM cell			7T SRAM cell			8T SRAM cell			9T SRAM cell		
	Average Power (in mW)	*Max. Power (in mW)*	*Min. Power (in mW)*	*Average Power (in mW)*	*Max. Power (in mW)*	*Min. Power (in mW)*	*Average Powe (in mW)*	*Max. Power (in mW)*	*Min. Power (in mW)*	*Average Power (in mW)*	*Max. Power (in mW)*	*Min. Power (in mW)*
180nm	3.06022	8.28749	1.94378	1.59671	2.28418	1.28507	2.21373	6.86197	1.45321	1.31918	6.57190	0.92968
130nm	2.67677	3.79242	1.95841	0.15729	0.49341	0.00002	1.99853	5.81349	1.45816	0.10638	3.72833	0.00007
100nm	2.61316	3.82970	1.97433	0.16218	0.62642	0.00031	2.01359	8.07961	1.45412	0.12295	5.58127	0.00005

6 CONCLUSION

The power of SRAM cell is mainly dissipated by the charging and discharging of highly capacitive bit lines because of their full swing nature. Charge recycling scheme is used in this paper to reduce power consumption of SRAM while charging and discharging of highly capacitive bit lines. This paper find out an efficient, low power SRAM cell memory by comparative analysis of 64-bit low power SRAM cell designs by using charge recycling scheme on 180nm 130nm and 100nm CMOS technology respectively. Based on the results it is clearly observed that 9T SRAM cell consumes less power as compare to 6T, 7T and 8T SRAM cell designs using CR.

Charge recycling scheme holds good for 7T and 9T SRAM cell as compared to 6T and 8T SRAM cell.64-bit 9T SRAM cell covers large area on die as it consists of 624 transistors in which 216 transistors are PMOS and 408 transistors are NMOS while 64-bit 7T SRAM cell consists of 448 transistors in which 128 transistors are PMOS and 320 transistors are NMOS. Therefore, if the average power consumption also with the die area considers than 7T SRAM cell with CR performs well as compared to 9T SRAM cell but 9T SRAM cell shows better performance in terms of average power consumption than 6T, 7T, 8T SRAM cell designs.

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