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Analysis of Control Strategies for Diode Clamped Multilevel Inverter

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ABSTRACT: This paper presents the comparison of various Pulse Width Modulation (PWM) strategies for the three phase Diode Clamped Multi Level Inverter (DCMLI). The main contribution of this paper is the proposal of new modulation schemes with Variable Amplitude (VA) and various new schemes adopting the constant switching frequency and also variable switching frequency multicarrier control freedom degree combination concepts are developed and simulated for the chosen three phase DCMLI. The three phase DCMLI, is controlled in this paper with Sinusoidal PWM (SPWM) reference along with triangular carriers and analysis is made among both without carrier overlapping and with Carrier Overlapping (CO) techniques to choose the better strategy by performing simulation using MATLAB-SIMULINK. The variation of Total Harmonic Distortion (THD) and fundamental RMS output voltage is observed for various modulation indices. It is observed that among the various equal amplitude PWM strategies, COPWM-C provides less THD and higher RMS voltage. It is recognized that among the various variable amplitude PWM strategies, VACOPWM-C provides less THD and VACOPWM-B provides higher RMS voltage. By comparing the equal amplitude PWM strategies with the variable amplitude PWM strategies it is inferred that VACOPWM-C provides less THD and VACOPWM-B provides higher RMS voltage. It is also inferred that carrier overlapping techniques provides better results compared to the without carrier overlapping techniques.

KEYWORDS: SPWM, DCMLI, THD, COPWM.

1 INTRODUCTION

Multi Level Inverter (MLI) is a power electronic system that produces output voltage from several levels of DC input voltages. The attractive feature of this technology is mainly in the range of medium to high voltage application and offers a number of advantages when compared to the conventional two-level inverter. Ceglia et al [1] described a new multilevel inverter topology. Tehrani et al [2] made a detailed review on novel multilevel inverter model. Caballero et al [3] performed a study on new asymmetrical hybrid multilevel inverter. Ahmed et al [4] made a survey on new multilevel inverter topology with reduced number of switches. Sun et al [5] evaluated performance of multilevel inverter capable of power factor control with DC link switches. Boller et al [6] presented a survey on optimal pulse width modulation of a dual three level inverter system operated from a single DC link. Spencer et al [7] developed the study of multi sampled multilevel inverters to improve control performance. Najafi and Yatim [8] made a detailed review of design and implementation of a new multilevel inverter topology. Abdalla et al [9] carried out survey on multilevel DC link inverter and control algorithm to overcome the PV partial shading. Kangarlu and Babaei performed a survey on generalized cascaded multilevel inverter using series connection of sub multilevel inverters.

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2 MULTI LEVEL INVERTER

Multilevel inverters are used in power conversion system due to improved voltage and current waveforms. It is recently emerged as very important alternatives in high power medium voltage applications because of their advantage over the conventional one and their capability to reduce the undesirable harmonics. So that performance and efficiency of the system is improved. The concept of multilevel inverter is introduced with an aim to reduce switching losses and to obtain the output voltage with multiple steps to achieve the improved power quality and higher voltage capability. Multilevel inverters are used in high voltage AC motor drive, distributive generation, high voltage direct transmission as well as SVC applications.

The main concept of this inverter is to use diodes to limit the voltage stress on power devices. A DCMLI typically consists of (m-1) capacitors on the DC bus where m is the total number of positive, negative and zero levels in the output voltage. The order of numbering of the switches is Sa1, Sa2, Sa3, Sa4, Sa1', Sa2', Sa3' and Sa4'. The DC bus consists of four capacitors C1, C2, C3 and C4 acting as voltage divider. For a DC bus voltage Vdc, the voltage across each capacitor is Vdc/4 and voltage stress on each device is limited to Vdc/4 through clamping diode. The middle point of the four capacitors 'n' can be defined as the neutral point. The principle of diode clamping to DC link voltages can be extended to any number of voltage levels. Since the voltages across the semiconductor switches are limited by conduction of the diodes connected to the various DC levels, the inverter is called DCMLI. The switches are arranged into 4 pairs (Sa1,Sa1'), (Sa2,Sa2'), (Sa3,Sa3') and (Sa4,Sa4'). If one switch of the pair is turned ON, the complementary switch of the same pair must be OFF. The output phase voltage Van, Vbn, Vcn have five states: Vdc/2, Vdc/4, 0, - Vdc/4 and - Vdc/2. Four switches are triggered at any point of time to select the desired level in the five level DCMLI. Fig.1 shows a conventional three phase five level DCMLI.

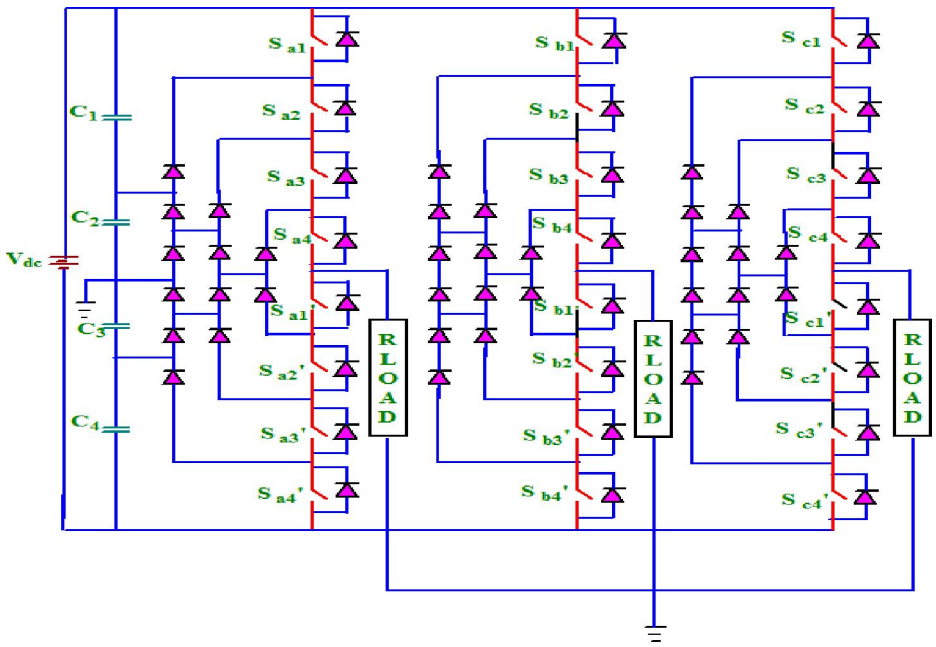

Fig. 1. Three phase five level DCMLI

3 MODULATION STRATEGIES

The most popular method of controlling the output voltage is by incorporating PWM control within the inverters. In this paper sixteen different modulation stragies are introduced in order to increase the output voltage and also to reduce the THD in which the fixed DC is converted into continuous AC signal efficiently by controlling the on and off time of PWM signal. It is generally recognized that, increasing the switching frequency of the PWM pattern results in reducing lower frequency harmonics. This paper includes reference waveform as sinusoidal and m-1 triangular carriers. The sixteen different modulation strategies are simulated in this work and the comparisons are made among them to chose the better technique which will be efficient and provides the output with improved power quality. The gate signals for chosen five level Diode Clamped Multilevel Inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a and for various PWM strategies. The simulation results presented in this work are compared and evaluated.

3.1 PHASE DISPOSITION PWM STRATEGY (PDPWM)

In this method all carriers have the same frequency, same amplitude and same phase but they are just different in DC offset to occupy contiguous bands. Since all carriers are selected with the same phase, this method is known as PD strategy. Carrier arrangement for this strategy is shown in Fig. 2.

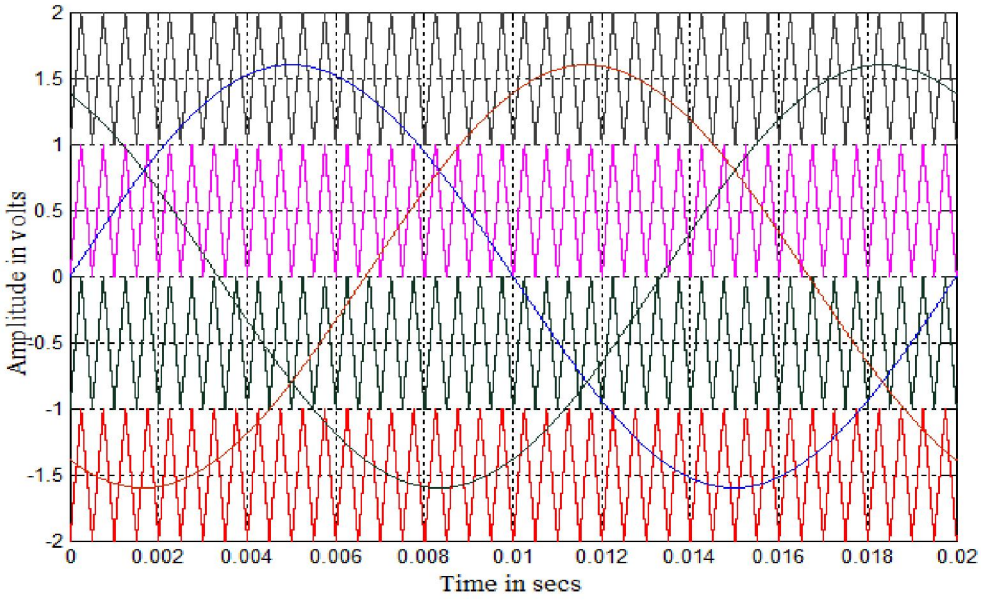

Fig. 2. Modulating and carrier waveforms for PDPWM strategy (m_a = 0.8 and m_f = 40)

3.2 VARIABLE AMPLITUDE PHASE DISPOSITION PWM STRATEGY (VAPDPWM)

This method is same as PDPWM method except that intermediate carriers are having variable amplitude compared to upper and lower carriers. Carrier arrangement for this scheme is shown in Fig. 3.

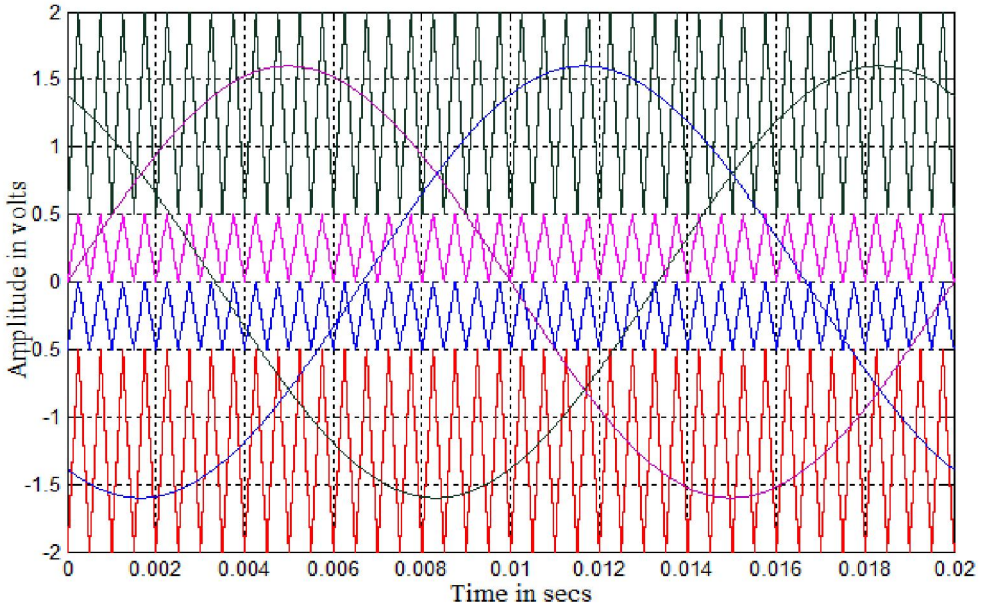

Fig. 3. Modulating and carrier waveforms for VAPDPWM strategy (m_a = 0.8 and m_f = 40)

3.3 PHASE OPPOSITION DISPOSITION PWM STRATEGY (PODPWM)

Four carriers, generated for five level inverter, is divided into two groups according to the positive and negative average levels. This scheme is similar to the PDPWM strategy but the two groups are opposite in phase with each other, so it is named as Phase Opposition Disposition PWM (PODPWM) technique. Carrier arrangement for this strategy is shown in Fig. 4.

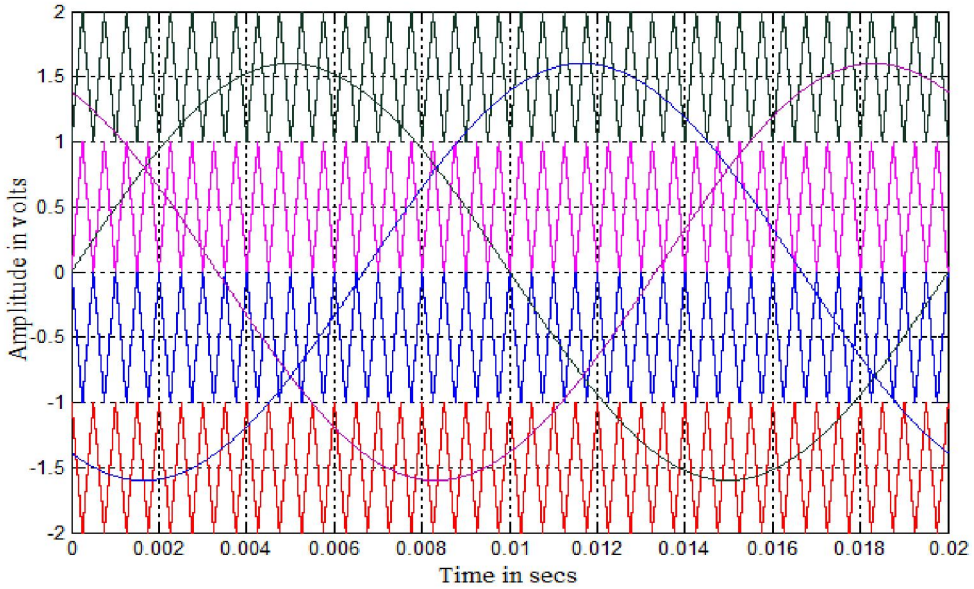

Fig. 4. Modulating and carrier waveforms for PODPWM strategy (m_a = 0.8 and m_f = 40)

3.4 VARIABLE AMPLITUDE PHASE OPPOSITION DISPOSITION PWM STRATEGY (VAPODPWM)

In this method four carriers, generated for five level inverter, is divided into two groups according to the positive and negative average levels. All carriers have the same frequency and varying amplitude, so it is named as Variable Amplitude Phase Opposition Disposition PWM strategy (VAPODPWM). Since all carriers are selected with the same phase, this method is similar to PODPWM strategy except with varying amplitude. It provides lower total harmonic distortion and relatively higher fundamental RMS voltage, while comparing to PDPWM technique. Carrier arrangement for this strategy is shown in Fig. 5.

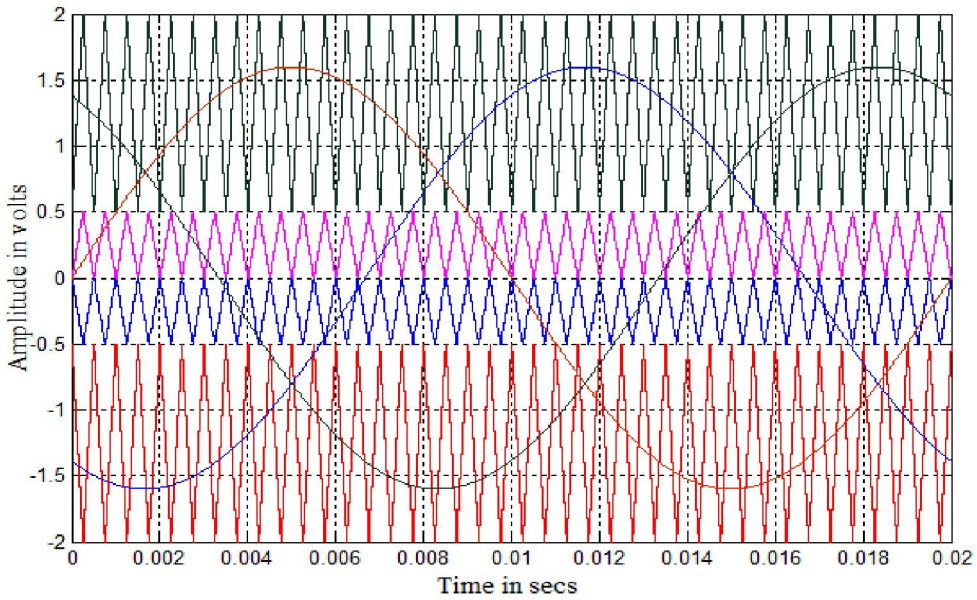

Fig. 5. Modulating and carrier waveforms for VAPODPWM strategy (m_a = 0.8 and m_f = 40)

3.5 ALTERNATE PHASE OPPOSITION DISPOSITION PWM STRATEGY (APODPWM)

In APOD strategy each carrier is phase shifted by 180 degrees from its adjacent one. In this strategy, carriers are seem to be invert their phase in turns from previous one and the same procedure is repeated below the zero average levels, hence it is named as Alternate Phase Opposition Disposition PWM (APODPWM) strategy. Carrier arrangement for this strategy is shown in Fig. 6.

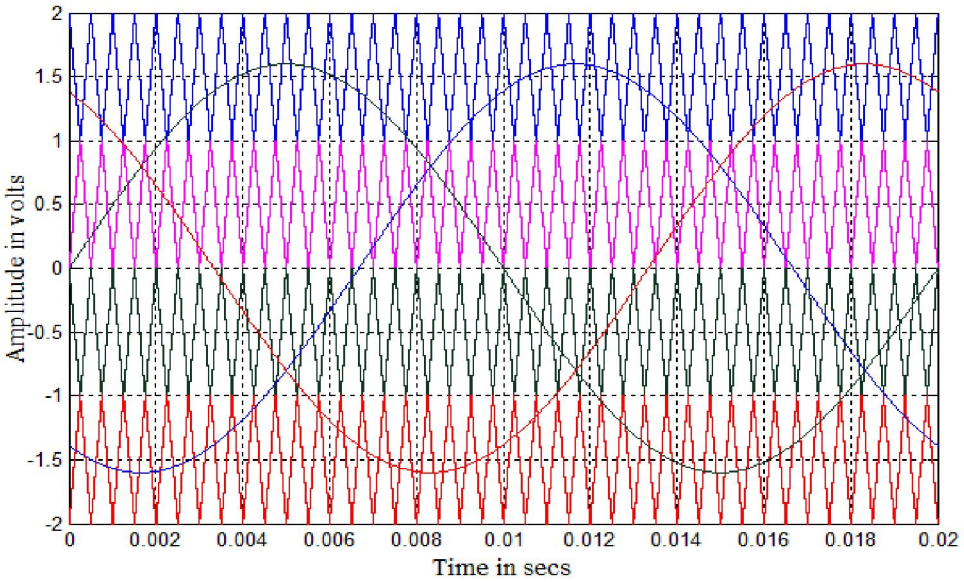

Fig. 6. Modulating and carrier waveforms for APODPWM strategy (m_a = 0.8 and m_f = 40)

3.6 VARIABLE AMPLITUDE ALTERNATE PHASE OPPOSITION DISPOSITION PWM STRATEGY (VAAPODPWM)

The VAAPODPWM is same as APODPWM method except that intermediate carriers are having variable amplitude compared to upper and lower carriers. In this strategy, carriers are seem to be invert their phase in turns from previous one and the same procedure is repeated below the zero average levels, hence it is named as Variable Amplitude Alternate Phase Opposition Disposition PWM (VAAPODPWM) strategy. Carrier arrangement for this strategy is shown in Fig. 7.

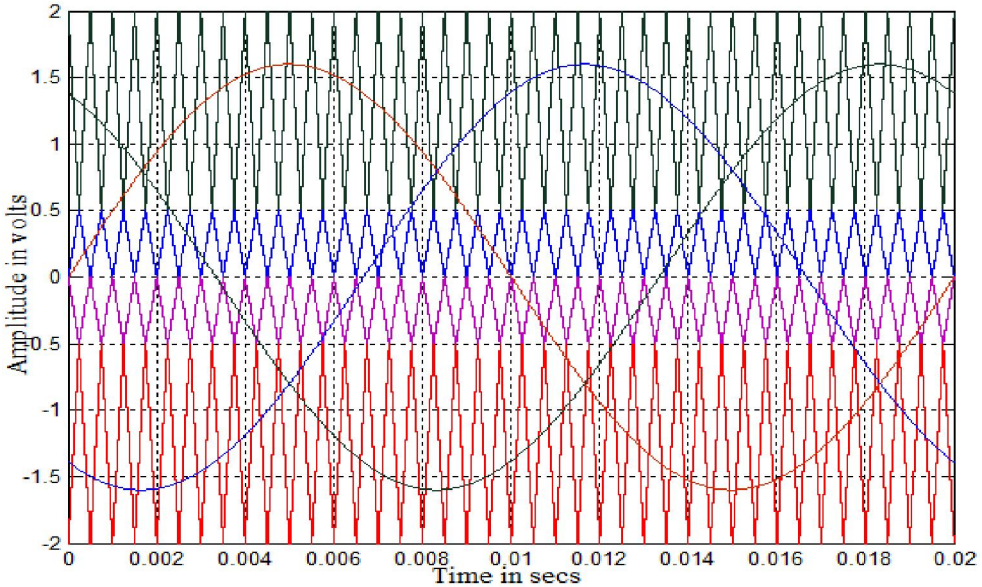

Fig. 7. Modulating and carrier waveforms for VAAPODPWM strategy (m_a = 0.8 and m_f = 40)

3.7 VARIABLE FREQUENCY PWM STRATEGY (VFPWM)

The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches. In order to equalize the number of switching for all the switches, variable frequency PWM strategy is used, in which the carrier frequency of the intermediate switches is properly increased to balance the number of switching for all the switches. Carrier arrangement for this strategy is displayed in Fig. 8.

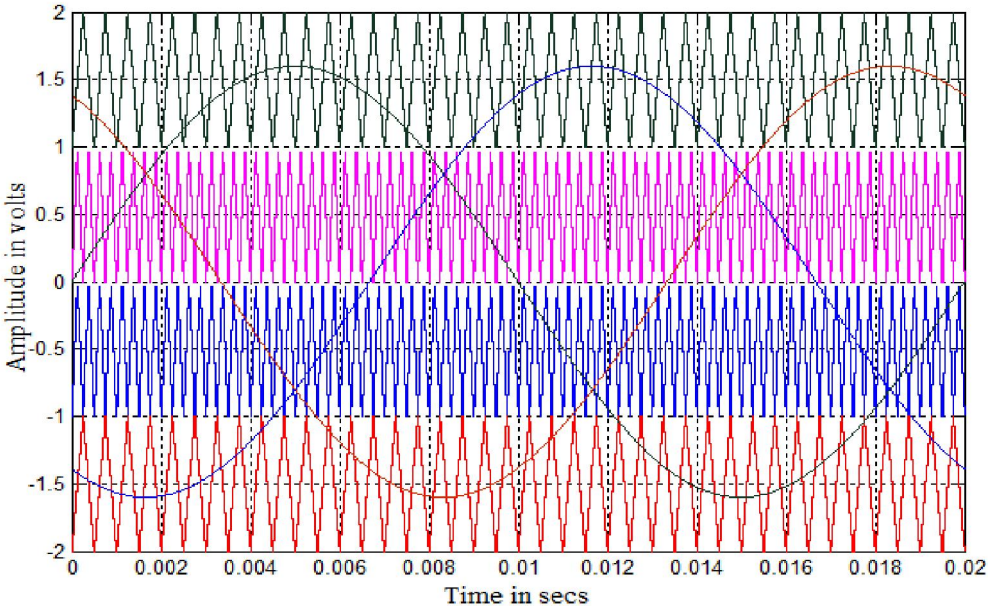

Fig. 8. Modulating and carrier waveforms for VFPWM strategy (m_a = 0.8 and m_f = 40 for upper switches and m_a = 0.8 and m_f = 80 for intermediate switches)

3.8 VARIABLE AMPLITUDE VARIABLE FREQUENCY PWM STRATEGY (VAVFPWM)

This VAVFPWM is same as VFPWM method except that intermediate carriers are having variable amplitude compared to upper and lower carriers. Carrier arrangement for this strategy is shown in Fig. 9.

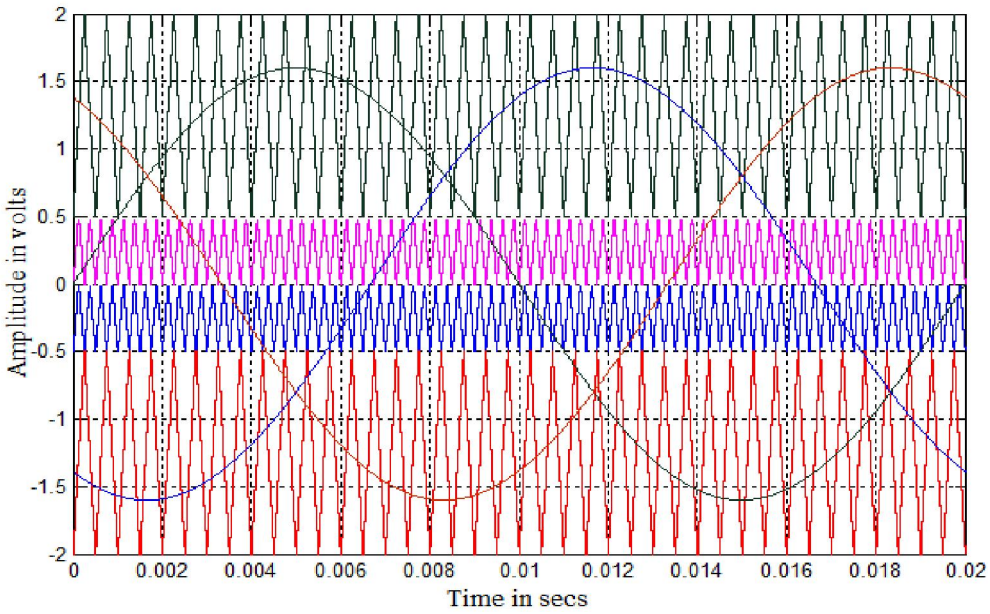

Fig. 9. Modulating and carrier waveforms for VAVFPWM strategy (m_a = 0.8 and m_f = 40 for upper switches and m_a = 0.8 and m_f = 80 for intermediate switches)

3.9 CARRIER OVERLAPPING PWM-A STRATEGY (COPWM-A)

In this method all carriers have the same frequency, same amplitude and same phase. Carriers needed for m level inverters is m-1, here we present four triangular overlapping carriers with one sine reference for five level inverter. All carriers, selected above and below the zero reference are in same phase and amplitude of each carrier chosen as 1.6 and overlapping amplitude will be $0.8(A_c/2)$, where A_c is overlapping amplitude of the carrier. Carrier arrangement for this strategy is shown in Fig. 10.

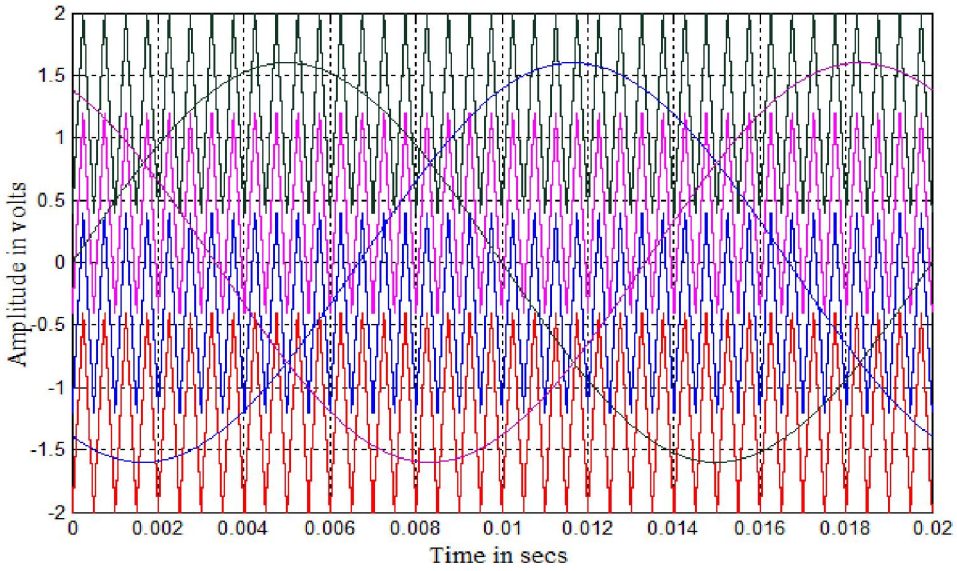

Fig. 10. Modulating and carrier waveforms for COPWM-A strategy (m_a = 0.8 and m_f = 40)

3.10 VARIABLE AMPLITUDE CARRIER OVERLAPPING PWM-A STRATEGY (VACOPWM-A)

In this method all carriers have the same frequency, same phase and varying amplitude, so it is named as Variable Amplitude Carrier Overlapping Pulse Width Modulation A strategy (VACOPWM-A). Since all carriers are selected with the same phase, this method is similar to COPWM-A strategy except with varying amplitude and overlapping amplitude is 0.8. It provides lower total harmonic distortion and relatively higher fundamental RMS voltage, while comparing to COPWM-A technique. Carrier arrangement for this strategy is shown in Fig. 11.

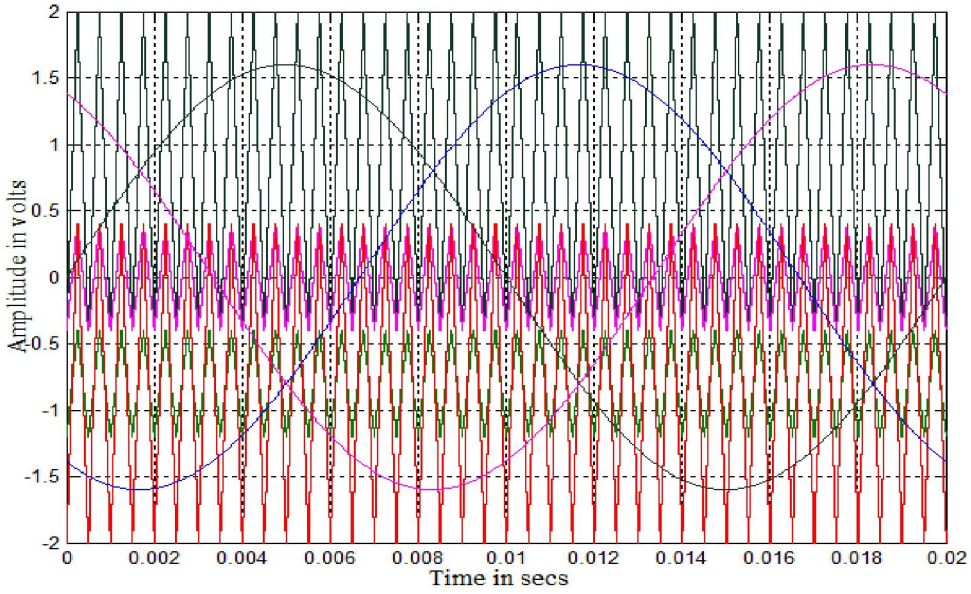

Fig. 11. Modulating and carrier waveforms for VACOPWM-A strategy (m_a = 0.8 and m_f = 40)

3.11 CARRIER OVERLAPPING PWM-B STRATEGY (COPWM-B)

Four carriers generated for five level inverter, is divided into two groups according to the positive and negative average levels. This scheme is similar to the COPWM-A strategy but the two groups are opposite in phase with each other with overlapping amplitude of 0.8, so it is named as Carrier Overlapping Pulse Width Modulation B (COPWM-B) technique. Carrier arrangement for this strategy is shown in Fig. 12.

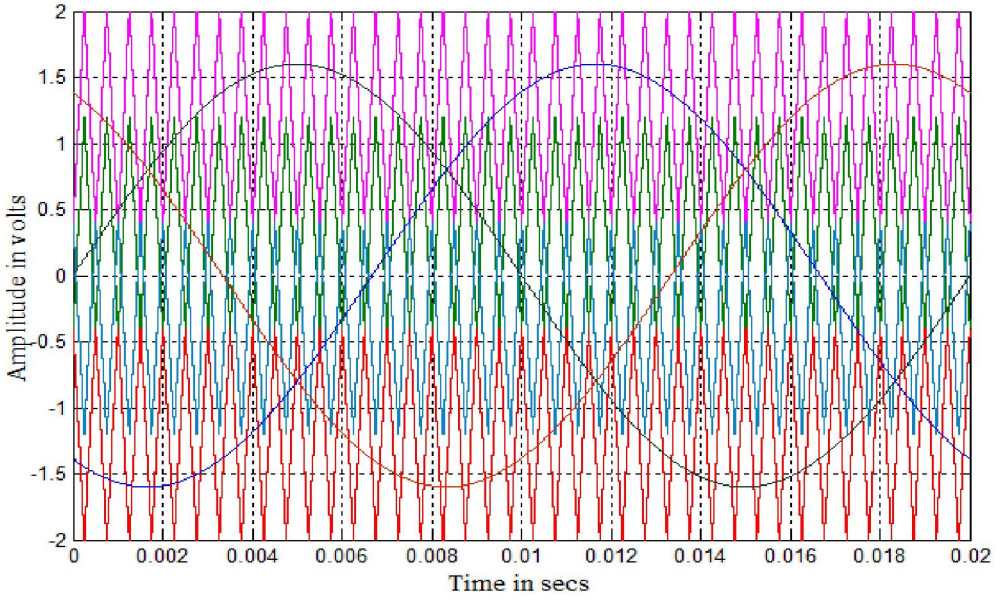

Fig. 12. Modulating and carrier waveforms for COPWM-B strategy (m_a = 0.8 and m_f = 40)

3.12 VARIABLE AMPLITUDE CARRIER OVERLAPPING PWM-B STRATEGY (VACOPWM-B)

In this scheme carriers are divided into two average levels according to the positive and negative groups, above and below the zero reference line with varying amplitude such that the two groups are opposite in phase with each other with an overlapping amplitude of 0.8. So, it is named as Variable Amplitude Carrier Overlapping Pulse Width Modulation B (VACOPPWM-B) strategy. Carrier arrangement for this strategy is shown in Fig. 13.

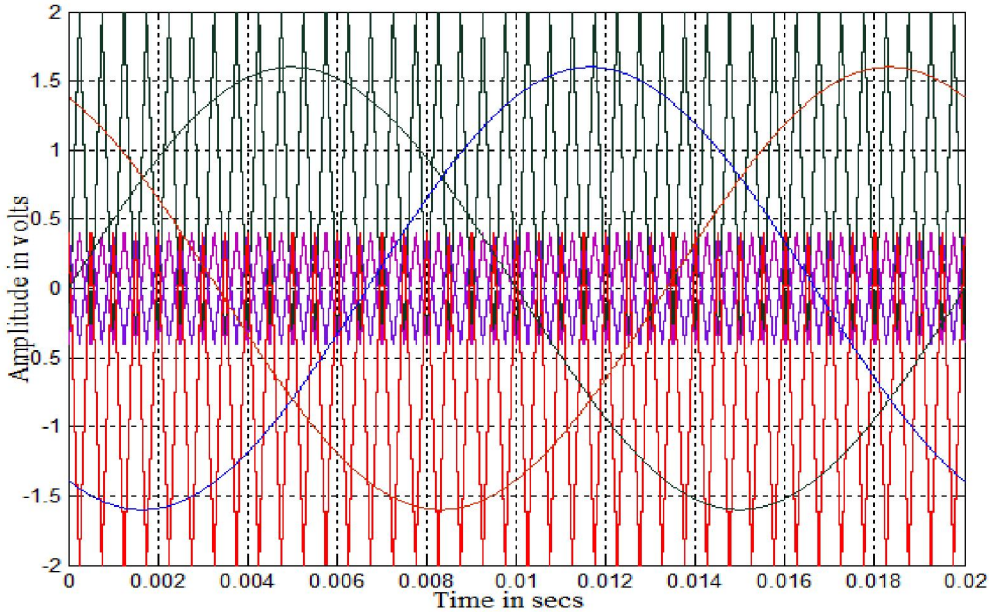

Fig. 13. Modulating and carrier waveforms for VACOPWM-B strategy (m_a = 0.8 and m_f = 40)

3.13 CARRIER OVERLAPPING PWM-C STRATEGY (COPWM-C)

In this strategy, carriers are seem to be invert their phase in turns from previous one and the same procedure is repeated below the zero average levels, with overlapping amplitude of 0.8, hence it is named as Carrier Overlapping Pulse Width Modulation C (COPWM-C)strategy. Carrier arrangement for this strategy is shown in Fig. 14.

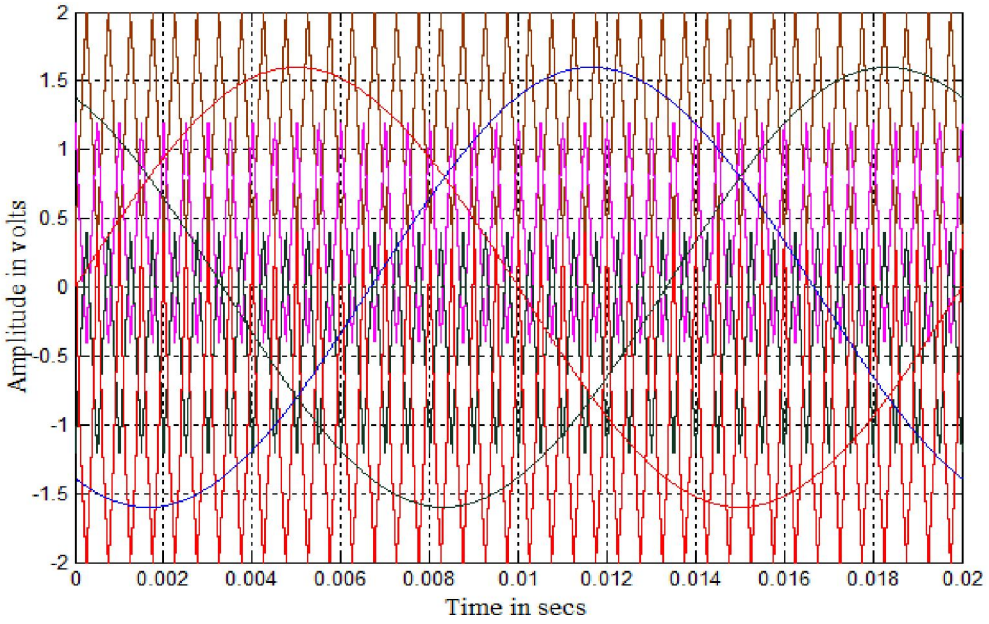

Fig. 14. Modulating and carrier waveforms for COPWM-C strategy (m_a = 0.8 and m_f = 40)

3.14 VARIABLE AMPLITUDE CARRIER OVERLAPPING PWM-C STRATEGY (VACOPWM-C)

In this pattern, carriers invert their phase from the previous one with same frequency and varying amplitude with overlapping amplitude of 0.8. So it named as Variable Amplitude Carrier Overlapping Pulse Width Modulation C (COPWM-C) strategy. Carrier arrangement for this strategy is shown in Fig. 15.

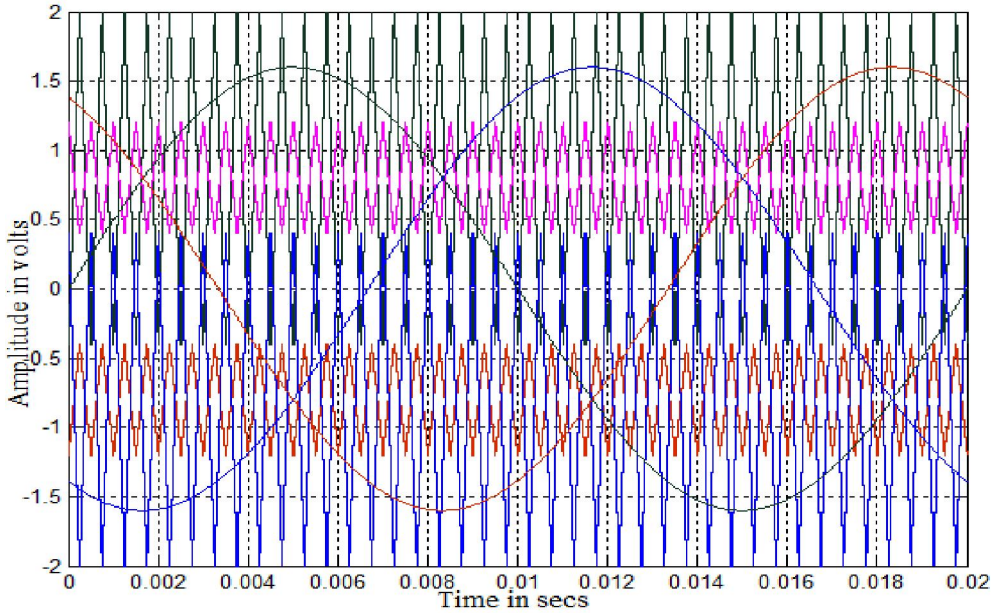

Fig. 15. Modulating and carrier waveforms for VACOPWM-C strategy (m_a = 0.8 and m_f = 40)

3.15 CARRIER OVERLAPPING PWM-D STRATEGY (COPWM-D)

This pattern is similar to COPWM-C scheme, such that the frequency of the intermediate carriers is increased for balancing the switching pattern for all switches and carriers are seem to be crossing the zero reference line with overlapping amplitude of 0.8. Carrier arrangement for this strategy is shown in Fig. 16.

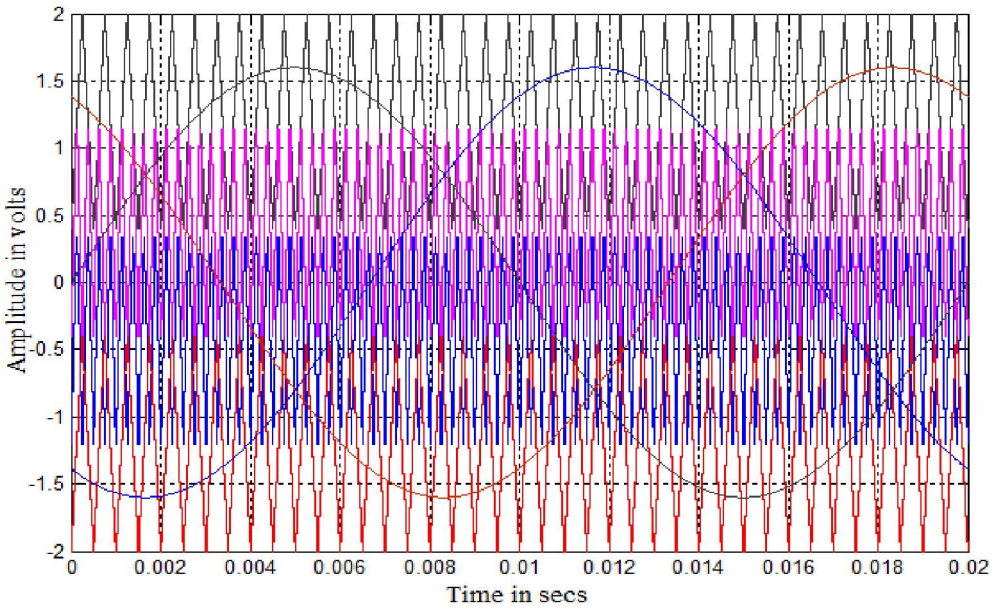

Fig. 16. Modulating and carrier waveforms for COPWM-D strategy (m_a = 0.8 and m_f = 40 for upper switches and m_a = 0.8 and m_f = 80 for intermediate switches)

3.16 VARIABLE AMPLITUDE CARRIER OVERLAPPING PWM-D STRATEGY (VACOPWM-D)

In order to balance the switching pattern for all switches, VACOPWM-D is introduced with overlapping amplitude of 0.8 and by increasing frequency of the intermediate carriers. Carrier arrangement for this strategy is shown in Fig. 17.

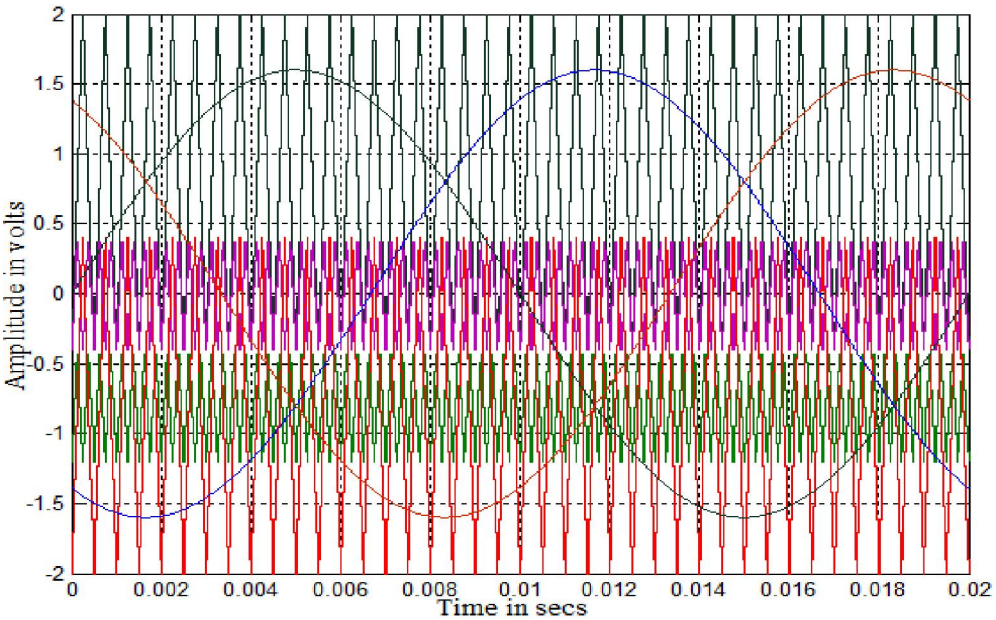

Fig. 17. Modulating and carrier waveforms for COPWM-D strategy (m_a = 0.8 and m_f = 40 for upper switches and m_a = 0.8 and m_f = 80 for intermediate switches)

4 SIMULATION RESULTS

Simulation studies are performed by using MATLAB-SIMULINK to verify the proposed PWM strategies for chosen three phase diode clamped five level inverter for various values of m_a ranging from 0.6 – 1 and corresponding %THD values are measured using FFT block and they are shown in Table 1&2. Table 3&4 shows the V_{RMS} of inverter output for the same modulation indices. Table 5&6. Shows the crest factor for different modulation indices which are measured using peak voltage and RMS voltage from FFT plots. Table 7&8. Shows form factor values which are calculated using RMS voltage and DC component from FFT plots. Table 9&10. Shows distortion factor for different modulation indices. From the analysis, it is inferred that PDPWM Strategy produces 30th, 32nd, 36th, 38th, and 40th harmonic energy. VAPD produces 3rd, 5th, 7th, 20th, 22nd, 24th, 32nd, 34th, 36th, 38th and 40th harmonic energy. POD Strategy produces 33rd,35th and 39th harmonic energy. VAPOD produces 3rd, 5th, 7th, 25th, 27th, 29th, 31st, 33rd, 37th and 39th harmonic energy. APOD produces 35th, 37th, and 39th harmonic energy. VAAPOD produces 3rd, 5th, 29th, 31st, 33rd, 35thand 39th harmonic energy. VF produces 34th, 38thand 40th harmonic energy. VAVF produces 3rd, 5th,7th,36th,38th,and 40th harmonic energy. COPWM-A produces 3rd, 38th and 40th harmonic energy. VACOPWM-A produces 3rd, 4th, 38th and 40th harmonic energy. COPWM-B produces 3rd, 35th, 37thand 39th harmonic energy. It is observed that the VACOPWM-B strategy produces significant 4th, 6th, 8th, 10th, 34th, 36th, 39th harmonic energy. It is observed that the COPWM-C strategy produces significant 2nd, 3rd, 4th, 5th, 33rd, 36th, 37th,38th, 39th and 40th harmonic energy. It is observed that the VACOPWM-C strategy produces significant 3rd, 5th, 7th, 16th, 20th, 29th, 31th, 33rd, 35th and 39th harmonic energy. COPWM-D produces 3rd, 36th, 38th and 40th harmonic energy. VACOPWM-D produces 2nd, 3rd, 4th, 5th and 39th harmonic energy. Figs.18-20 show the simulated output voltages of chosen DCMLI and the corresponding FFT plots are shown in Figs. 21-23 but only for one sample value of m_a = 0.8 and m_f = 40.

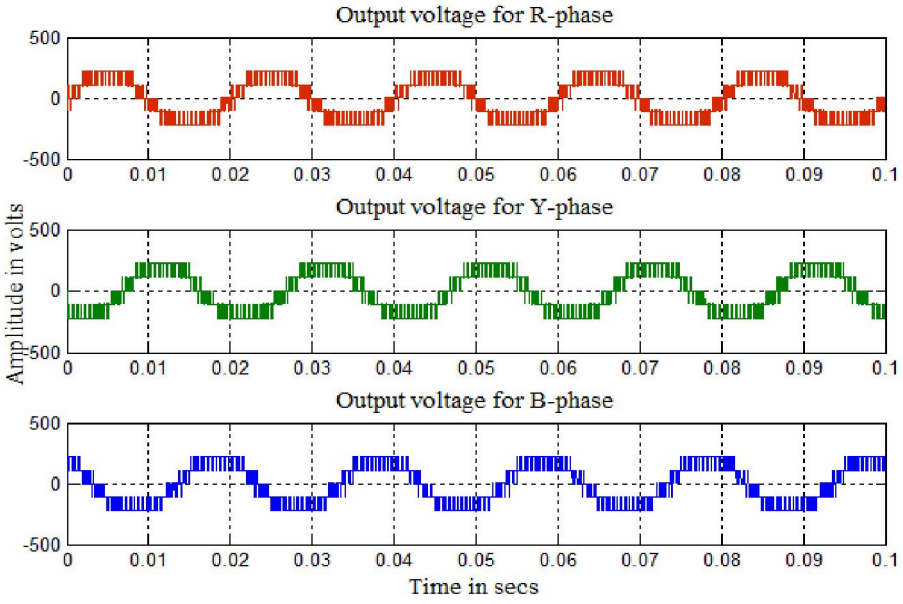

Fig. 18. Simulated output voltage generated by COPWM-C technique for R-load

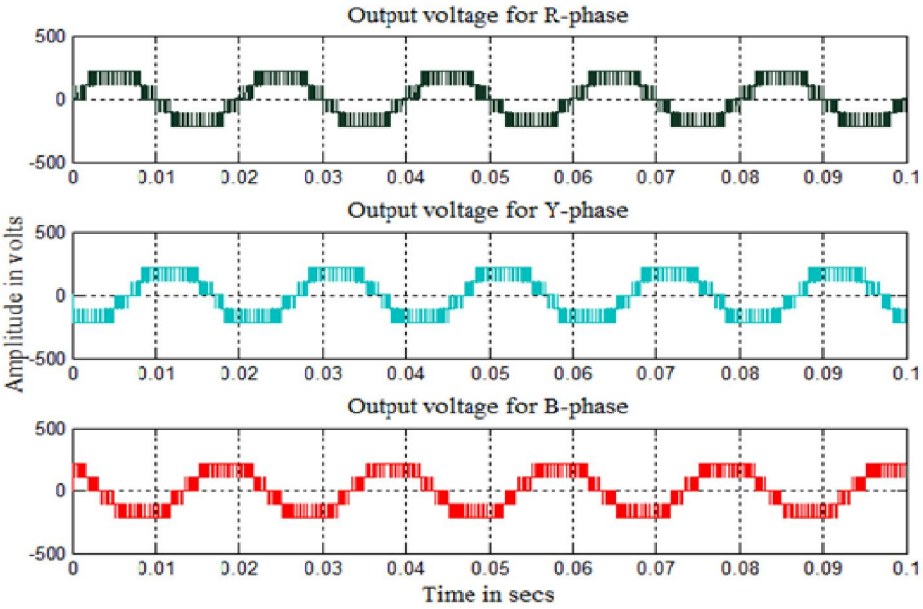

Fig. 19. Simulated output voltage generated by VACOPWM-C technique for R-load

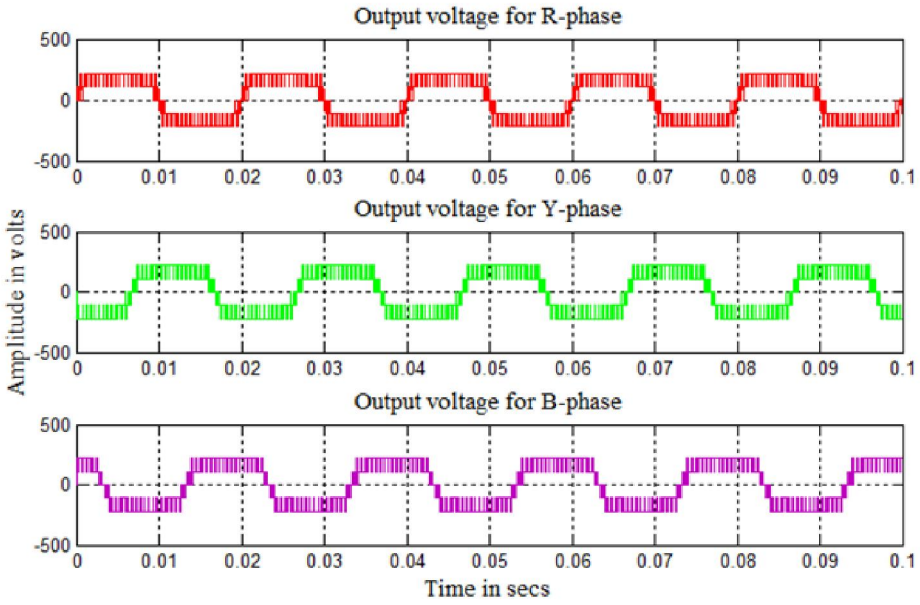

Fig. 20. Simulated output voltage generated by VACOPWM-B technique for R-load

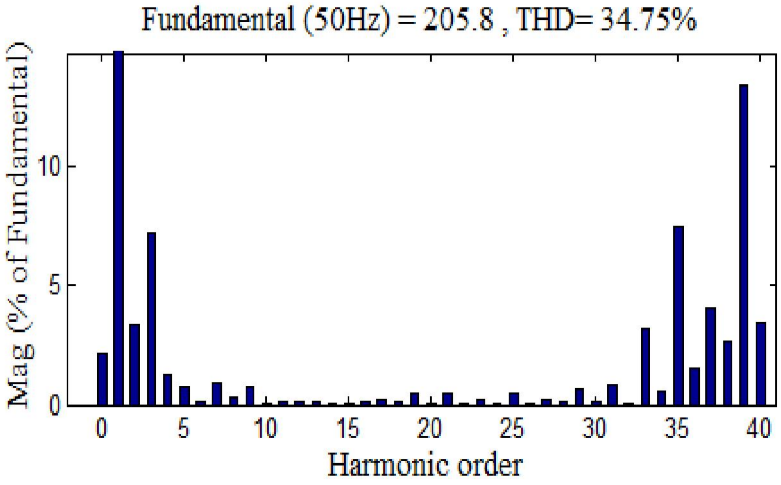

Fig. 21. FFT spectrum for COPWM –C technique

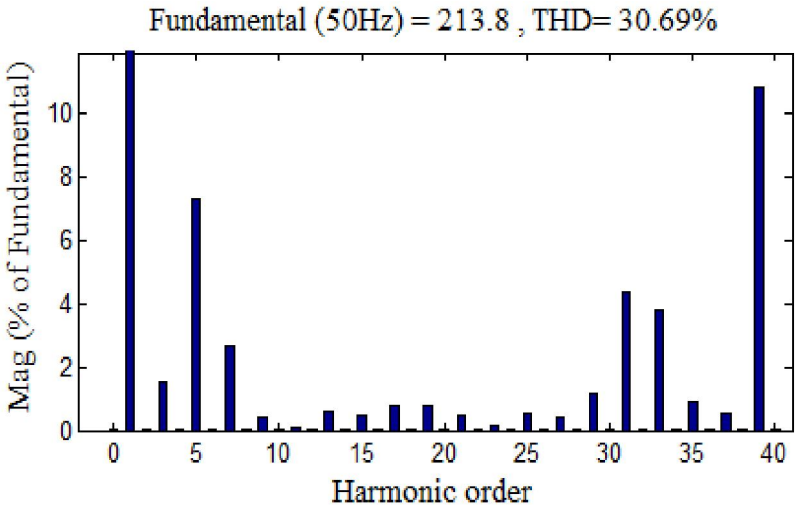

Fig. 22. FFT spectrum for VACOPWM –C technique

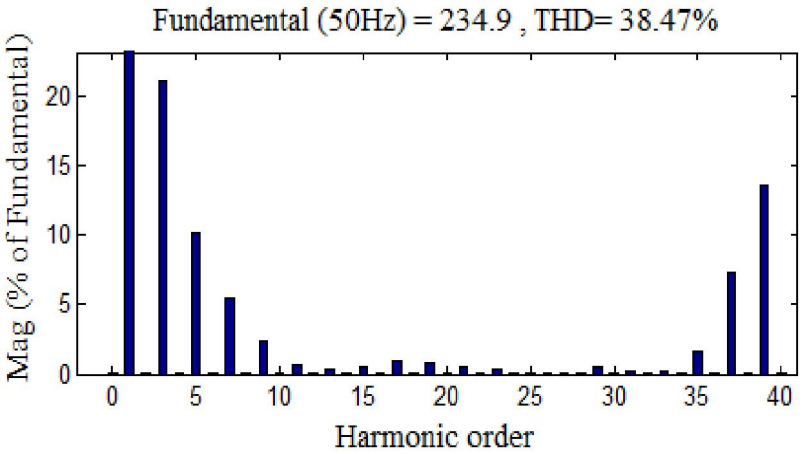

Fig. 23. FFT spectrum for VACOPWM –B technique

Table 1. %THD for Different Modulation Indices for Conventional PWM Strategy

m_a	PD	VAPD	POD	VAPOD	APOD	VAAPOD	VF	VAVF
1	27.05	27.87	26.95	27.70	26.54	27.43	27.09	27.97
0.9	33.63	32.01	33.51	31.99	33.22	31.57	33.48	32.19
0.8	38.39	35.57	38.15	35.17	38.16	35.57	38.34	35.57
0.7	42.09	38.29	41.90	38.01	41.99	37.88	42.51	38.88
0.6	44.48	39.85	44.54	39.59	44.57	39.76	44.54	39.94

Table 2. %THD for Different Modulation Indices with COPWM Strategy

m_a	COPWM-A	VA COPWM-A	COPWM-B	VA COPWM-B	COPWM-C	VA COPWM-C	COPWM-D	VA COPWM-D
1	33.57	37.46	31.78	33.71	26.54	24.61	31.94	33.94
0.9	38.51	41.58	36.82	36.51	30.67	27.67	36.81	37.78
0.8	43.73	45.34	41.91	38.47	34.75	30.69	42.08	40.90
0.7	50.28	49.88	47.85	40.95	37.64	34.15	47.29	44.67
0.6	58.88	57.66	56.28	42.21	40.75	39.34	55.57	50.14

Table 3. V_{RMS} for Different Modulation Indices for Conventional PWM Strategy

m_a	PD	VAPD	POD	VAPOD	APOD	VAAPOD	VF	VAVF
1	155.3	169	155.3	169.2	155.4	168.9	155.3	169
0.9	139.9	158.3	139.8	158.1	140.1	158.4	139.9	158.4
0.8	124.3	147.8	124.5	147.5	121.4	147.9	124.4	147.8
0.7	108.5	137	108.4	137.2	108.5	136.9	108.3	137.2
0.6	92.95	126.2	92.75	126.2	92.9	126.2	93.16	126.2

Table 4. V_{RMS} for Different Modulation Indices with COPWM Strategy

m_a	COPWM-A	VA COPWM-A	COPWM-B	VA COPWM-B	COPWM-C	VA COPWM-C	COPWM-D	VA COPWM-D
1	166.5	175	165.4	179.3	167	170.6	166.3	174.7
0.9	155.8	167	154.6	172.5	156.7	161	155.6	166.9
0.8	144.3	158.9	142.6	166.1	145.5	151.2	144.2	158.8
0.7	130.9	149.7	129.1	159.3	132.7	139.2	130.8	149.1
0.6	116.8	137.5	114.7	151.9	119.5	121.2	116.2	137

Table 5. Crest Factor for Different Modulation Indices for Conventional PWM Strategy

m_a	PD	VAPD	POD	VAPOD	APOD	VAAPOD	VF	VAVF
1	1.4140	1.4142	1.4140	1.4143	1.4144	1.4144	1.4140	1.4142
0.9	1.4138	1.4144	1.4148	1.4142	1.4139	1.4141	1.4138	1.4147
0.8	1.4143	1.4147	1.4144	1.4142	1.4139	1.4137	1.4139	1.4147
0.7	1.4147	1.4145	1.4142	1.4139	1.4147	1.4141	1.4136	1.4139
0.6	1.41473	1.4144	1.4145	1.4136	1.4144	1.4144	1.4136	1.4144

Table 6. Crest Factor for Different Modulation Indices with COPWM Strategy

m_a	COPWM-A	VA COPWM-A	COPWM-B	VA COPWM-B	COPWM-C	VA COPWM-C	COPWM-D	VA COPWM-D
1	1.4138	1.4142	1.4147	1.4143	1.4143	1.4144	1.4143	1.4144
0.9	1.4139	1.4137	1.4146	1.4144	1.4141	1.4142	1.4145	1.4144
0.8	1.4137	1.4140	1.4137	1.4142	1.4144	1.4140	1.4140	1.4143
0.7	1.4140	1.4141	1.4136	1.4155	1.4137	1.4137	1.4143	1.4138
0.6	1.4146	1.414	1.4137	1.4141	1.4138	1.4146	1.4144	1.4142

Table 7. Form Factor for Different Modulation Indices for Conventional PWM Strategy

m_a	PD	VAPD	POD	VAPOD	APOD	VAAPOD	VF	VAVF
1	2588.3	16900	15530	16920	15540	16890	1725.5	4225
0.9	1554.4	565.3	13980	15810	14010	15840	1554.4	7920
0.8	1381.1	328.44	INF	14750	INF	14790	1244	1055.7
0.7	417.3	913.3	INF	13720	INF	13690	984.5	6860
0.6	442.6	788.7	INF	12620	INF	12620	1863.2	1402.2

Table 8. Form Factor for Different Modulation Indices with COPWM Strategy

m_a	COPWM-A	VA COPWM-A	COPWM-B	VA COPWM-B	COPWM-C	VA COPWM-C	COPWM-D	VA COPWM-D
1	5550	29.711	295.35	17930	126.51	17060	5543.3	28.780
0.9	1731.1	22.939	214.72	17250	101.09	16100	2593.3	23.673
0.8	14430	18.563	156.70	16610	67.05	15120	14420	18.882
0.7	13090	14.449	91.560	15930	46.23	13920	467.14	13.831
0.6	16685	9.8004	87.557	15190	33.194	INF	528.18	9.6140

Table 9. Distortion Factor for Different Modulation Indices for Conventional PWM Strategy

m_a	PD	VAPD	POD	VAPOD	APOD	VAAPOD	VF	VAVF
1	0.0353	1.333	0.0400	1.3632	0.0222	1.3302	0.0732	1.3429
0.9	0.0472	1.3655	0.0677	1.3772	0.0319	1.3246	0.0352	1.3903
0.8	0.0368	1.4407	0.0556	1.3773	0.055	1.4328	0.085	1.4307
0.7	0.0942	1.486	0.0296	1.5906	0.0224	1.4697	0.0647	1.5145
0.6	0.0425	1.473	0.0366	1.4619	0.0288	1.4815	0.0857	1.4819

Table 10. Distortion Factor for Different Modulation Indices with COPWM Strategy

m_a	COPWM-A	VA COPWM-A	COPWM-B	VA COPWM-B	COPWM-C	VA COPWM-C	COPWM-D	VA COPWM-D
1	0.838	3.022	0.768	2.276	1.109	0.941	0.823	3.038
0.9	0.741	3.382	0.681	2.336	5.589	0.628	0.730	3.266
0.8	0.569	3.576	0.485	2.384	1.154	0.344	0.542	3.488
0.7	0.247	3.976	0.209	2.436	1.076	0.419	0.226	3.832
0.6	0.052	3.977	0.085	2.352	1.073	1.082	0.137	3.938

5 CONCLUSION

In this paper various new schemes of Pulse Width Modulation Strategies are developed and simulated for chosen three phase DCMLI. Performance indices like %THD, V_{RMS} (indicating the amount of DC bus utilization), Crest Factor (CF) and Form Factor (FF) related to power quality issues have been evaluated, presented and analyzed. The variation of Total Harmonic Distortion (THD) in the inverter output voltage is observed for various modulation indices. It is observed that among the various equal amplitude PWM strategies, COPWM-C provides less THD and higher RMS voltage. It is recognized that among the various variable amplitude PWM strategies, VACOPWM-C provides less THD and VACOPWM-B provides higher RMS voltage. By comparing the equal amplitude PWM strategies with the variable amplitude PWM strategies it is inferred that VACOPWM-C provides less THD and VACOPWM-B provides higher RMS voltage. The result indicate that appropriate PWM strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).

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