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Studies on Unipolar Inverted Sine Carrier PWM Strategies for Three Phase Five Level Cascaded Inverter

C.R.Balamurugan[1], S.P.Natarajan[2], and R.Bensraj[3]

[1]Department of EEE,
Arunai Engineering College,
Tiruvannamalai, Tamilnadu, India

[2]Department of EIE,
Annamalai University,
Chidambaram, Tamilnadu, India

[3]Department of EEE,
Annamalai University,
Chidambaram, Tamilnadu, India

ABSTRACT: This paper presents the comparison of Unipolar Inverted Sine Carrier Pulse Width Modulation (UISCPWM) techniques for the Cascaded Multi Level Inverter (CMLI). Due to switch combination redundancies, there are certain degrees of freedom to generate the multilevel AC output voltage. This paper presents the use of Control Freedom Degree (CFD) combination. The effectiveness of the pulse width modulation strategies developed using CFD are demonstrated using simulation. The results indicate that the chosen five level inverter triggered by the developed UISC phase shift PWM and UISC variable frequency PWM strategy with sine and stepped wave references and UISC alternate phase opposition disposition PWM strategy with 60 degree reference exhibit reduced harmonics and UISC carrier overlapping PWM provides higher fundamental RMS output voltage for all three chosen references. Simulations are performed using MATLAB-SIMULINK.

KEYWORDS: ISCPWM, CMLI, THD, 60 degree, FF, unipolar.

1 INTRODUCTION

The multilevel inverter topology gives the advantages of usage in high power and high voltage application with reduced harmonic distortion without a transformer. The semiconductor devices are connected in series to form one single high-voltage switch in which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Peng [1] proposed a generalized multilevel inverter topology with self voltage balancing. Rodriguez et al [2] made a survey on topologies , control and applications of multilevel inverter. Corzine et al [3] analysed control of cascaded multilevel inverter. Jeevananthan et al proposed inverted sine carrier for fundamental fortification in PWM inverters and FPGA based implementation [4]. Rajesh Gupta et al [5] developed switching characteristics of cascaded multilevel inverter controlled systems. Malinowski [6] also made a detailed survey on cascaded multilevel inverter. Seyezhai and Mathur [7] developed hybrid multilevel inverter using ISPWM technique for fuel cell applications. Abhisek maiti et al [8] developed a microcontroller based inverted sine PWM switching technique for single phase inverter. Seyezhai and Mathur [9] suggested inverted sine pulse width modulated three phase cascaded multilevel inverter. Bensraj and Natarajan proposed unipolar PWM using trapezoidal amalgamated rectangular function for improved performance of MLI as in [10]. Urmila and Subbarayudu [11] undertook comparative study of various pulse width modulation techniques. This paper discusses a

Corresponding Author: S.P.Natarajan (spn_annamalai@rediffmail.com)

comparative study carried out on various new unipolar strategies for chosen five level CMLI. Simulations are performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

2 MULTILEVEL INVERTER

A cascaded multilevel inverter consists of a series of H-bridge inverter units. The general function of this inverter is to synthesize a desired voltage from several Separate DC Sources (SDCSs). The concept of this inverter is based on connecting output H-bridge inverter cells in series to get a sinusoidal load voltage. The load voltage is the sum of the voltage that is generated by each cell. The number of load voltage levels are 2*n*+1 where *n* is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components compared to the diode clamped or the flying capacitor so the price and the weight of the inverter is less than that of the two former types. Fig. 1 shows a configuration of the three phase five level cascaded multilevel inverter.

The load voltage is equal to the summation of the output voltage of the respective modules that are connected in series. The number of modules (n) which is equal to the number of DC sources required depend on the total number of positive, negative and zero levels (m) of the CMLI. It is usually assumed that m is odd as this would give an integer valued n. In this work, load voltage consists of five levels which include $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$ and $-2V_{DC}$ and the number of modules needed is 2. The following equation gives the relation between n and m; n = (m-1)/2.

The gate signals for chosen five level cascaded inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a and for various PWM strategies. Fig. 2 shows a sample SIMULINK model developed for UISC phase disposition PWM method. The simulation results presented in this work in the form of the outputs of the chosen MLI are compared and evaluated.

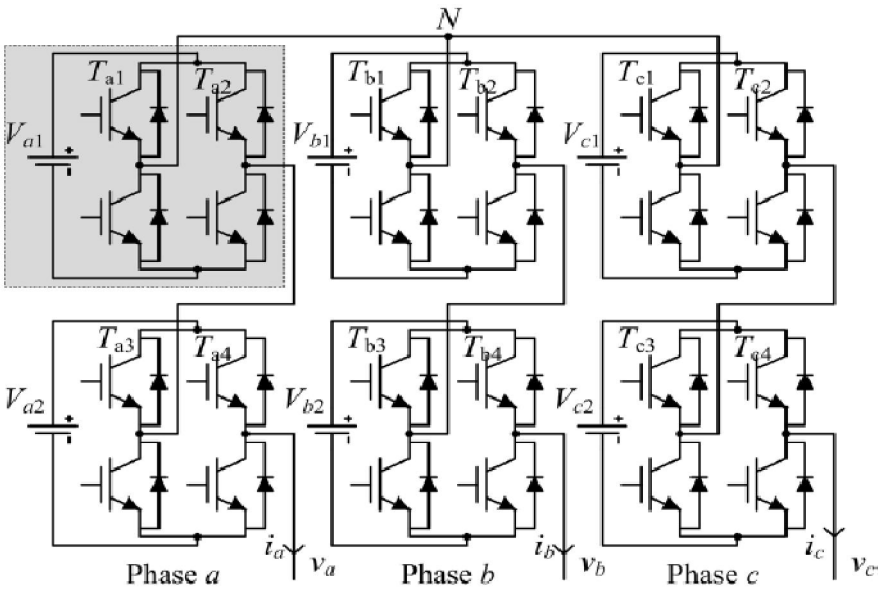

Fig. 1. Three Phase Cascaded Five Level Inverter

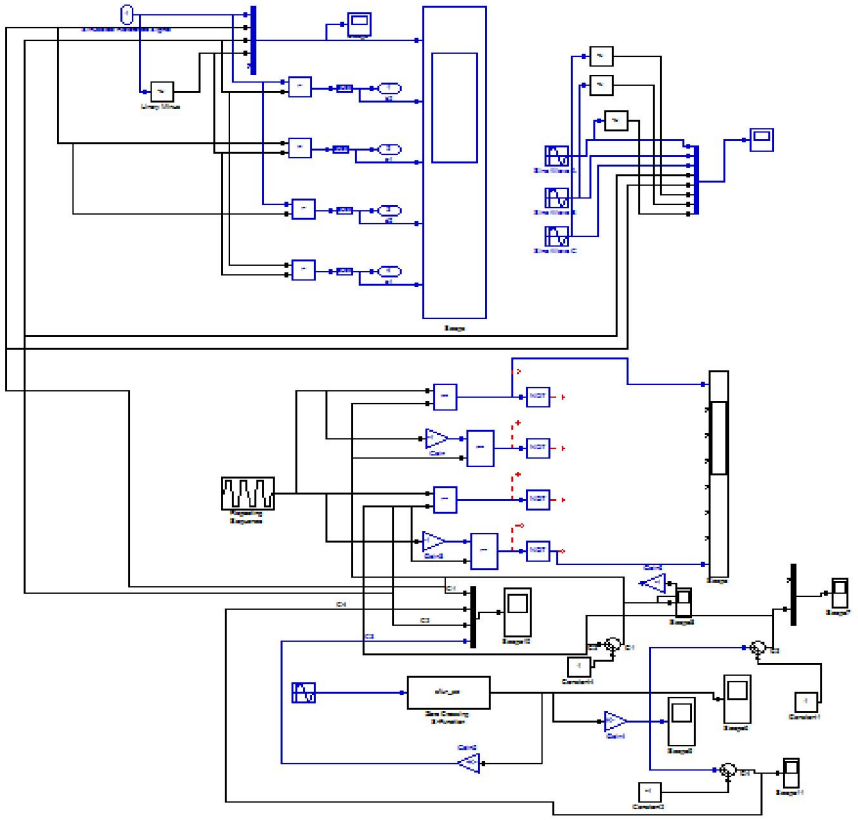

Fig. 2. Sample PWM Generation Logic Developed Using SIMULINK for UISC Phase Disposition PWM Technique

3 UNIPOLAR MULTICARRIER PWM STRATEGIES WITH SINE REFERENCE

This paper presents four types of unipolar PWM strategies. The reference in the unipolar strategy may be a rectified sinusoid or two sine references (sine and 180^0 phase shifted sine) The later is used in this work. The multi carriers are positioned above zero level.

For an m level inverter using unipolar multi carrier technique, (m-1)/2 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and it is placed at the zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on [10]. Otherwise, the device switches off. The frequency ratio m_f is defined in the unipolar PWM strategy as follows:

$$m_f = \frac{f_c}{f_m}$$

In this paper, m_f = 40 and m_a is varied from 0.6 to 1.

m_f is chosen as 40 as a trade off in view of the following reasons:

(i) to reduce switching losses (which may be high at large m_f)
(ii) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies.
(iii) to effectively utilise the available dSPACE system for hardware implementation.

The Inverted Sine Carrier PWM (ISCPWM) method uses the conventional sinusoidal reference signal and inverted sine carriers. The control scheme uses the inverted sine carrier since it that helps to maximize the output voltage for a given modulation index. The pulses are generated when the amplitude of the modulating signal is greater than that of the carrier signal[4].

The advantages of ISCPWM method are:

(i) It has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM without any pulse dropping.
(ii) The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges.

(iii) There is reduction in the total harmonic distortion and switching losses.
(iv) The appreciable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required.
(v) To increase the fundamental amplitude in the sinusoidal pulse width modulation the only way is by increasing the modulation index beyond 1 which is called over modulation. Over modulation causes the output voltage to contain many lower order harmonics and also makes the fundamental component V_s modulation index relation non-linear. Inverted sine pulse width modulation technique replaces over modulation.

This paper focuses on inverted sine carrier based sinusoidal PWM strategies, 60 degree PWM and stepped wave PWM strategies which have been developed for the chosen three phase cascaded MLI.

3.1 Unipolar Inverted Sine Carrier Phase Disposition PWM (UISCPDPWM) Strategy

The principle of the UISCPDPWM strategy is to use several inverted sine carriers with two modulation waves. For an m level inverter, (m-1)/2 carriers of the same frequency f_c and the same peak-to-peak amplitude A_c are disposed so that the bands they occupy are contiguous [10]. The carrier set is placed above the zero reference.

$$m_a = \frac{A_m}{(n*A_c)}$$

where n is the number of carriers.

Carrier arrangements for five level UISCPDPWM are shown in Fig. 3 for m_a=0.8.

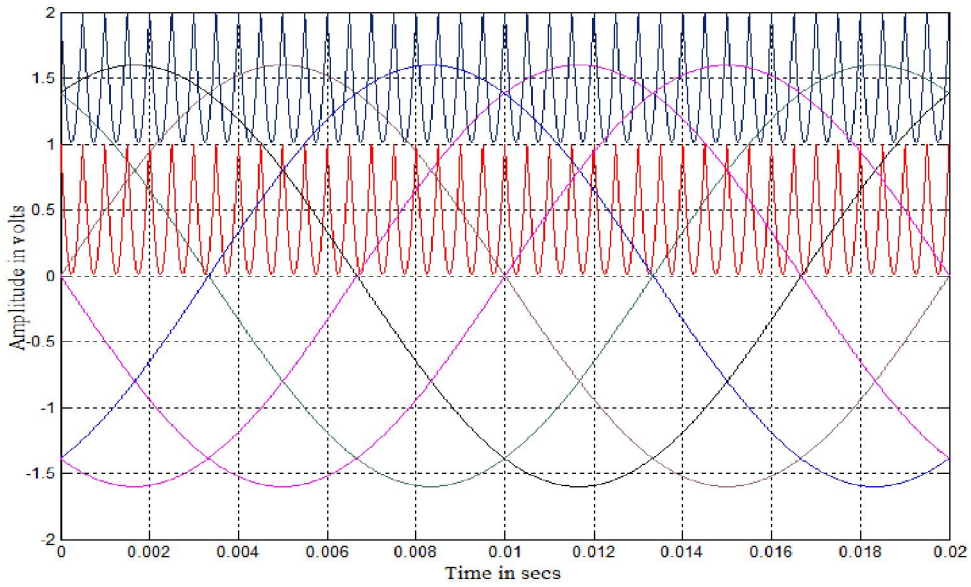

Fig. 3. Carrier Arrangements for UISCPDPWM Strategy (m_a = 0.8 , m_f = 40)

3.2 Unipolar Inverted Sine Carrier Alternative Phase Opposition And Disposition PWM (UISCAPODPWM) Strategy

This APOD strategy requires each of the two carrier waves in the upper half side for a inverter to be phase displaced from each other by 180 degrees alternately.

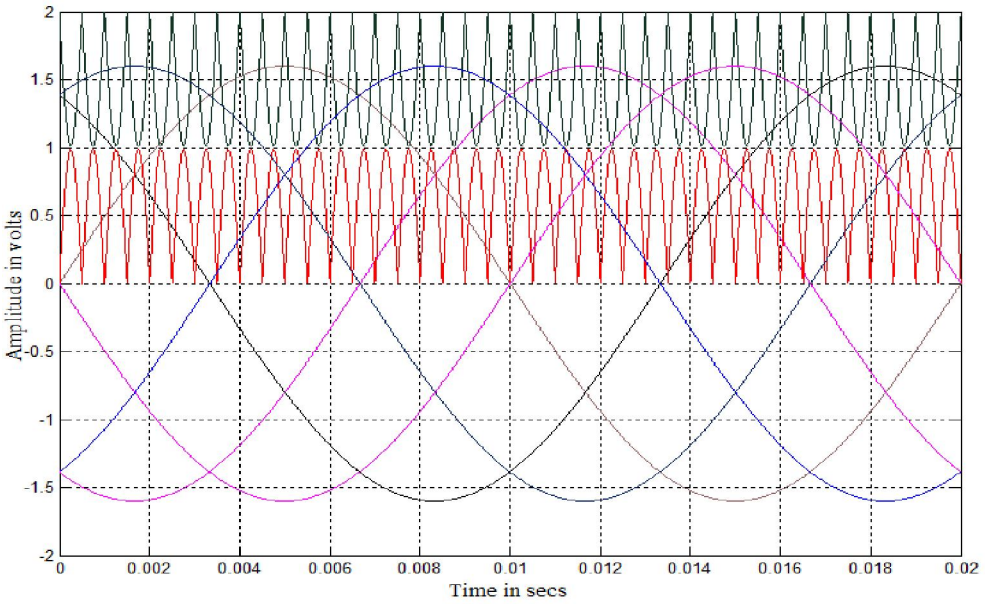

Fig. 4. Carrier Arrangements for UISCAPODPWM Strategy ($m_a = 0.8$, $m_f = 40$)

3.3 UNIPOLAR INVERTED SINE CARRIER PHASE SHIFT PWM (UISCPSPWM) STRATEGY

The UISCPSPWM uses two carrier signals of same amplitude and frequency which are phase shifted by 90^0 to one another to generate the five level inverter output voltage. The gate signals for the CMLI are derived by comparison of the carriers with two sinusoidal references. The amplitude modulation index is defined for this strategy as follows:

$$m_a = \frac{A_m}{A_c}$$

Carriers for five level inverter with UISCPSPWM strategy are illustrated in Fig. 5 for m_a=0.8.

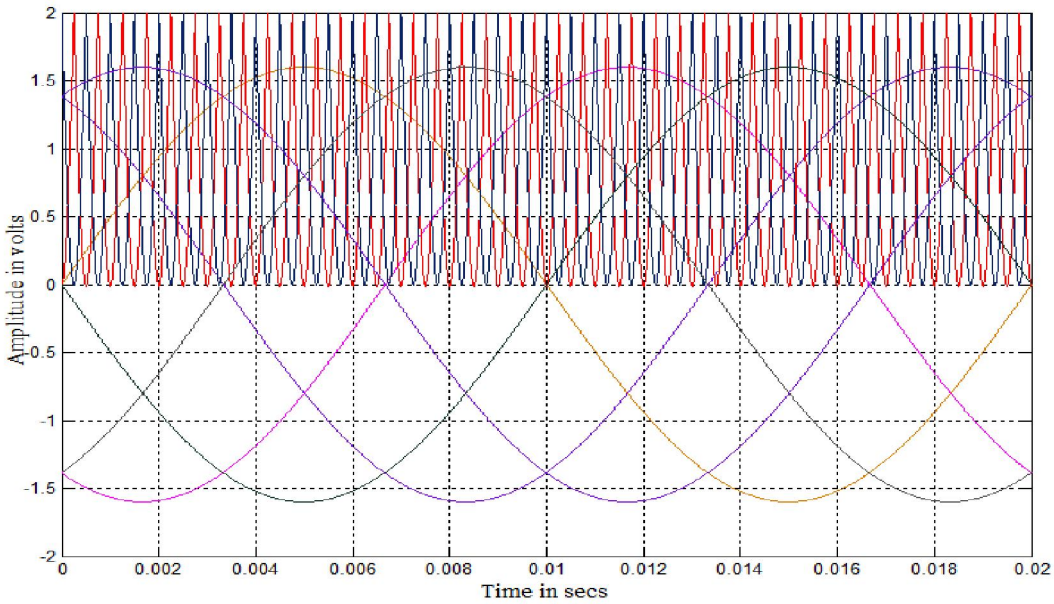

Fig. 5. Carrier Arrangements for UISCPSPWM Strategy ($m_a = 0.8$, $m_f = 40$)

3.4 UNIPOLAR INVERTED SINE CARRIER CARRIER OVERLAPPING PWM (UISCCOPWM) STRATEGY

The UISCCOPWM has two carriers signals of peak-to-peak amplitude A_c and they overlap with each other. The gate signals for this strategy are derived by comparing the two overlapping carriers with the two sine references [10]. Fig. 6 shows the carrier arrangements for the chosen MLI with UISCCOPWM strategy.

$$m_a = \frac{A_m}{\left(\frac{m}{4}\right) A_c}$$

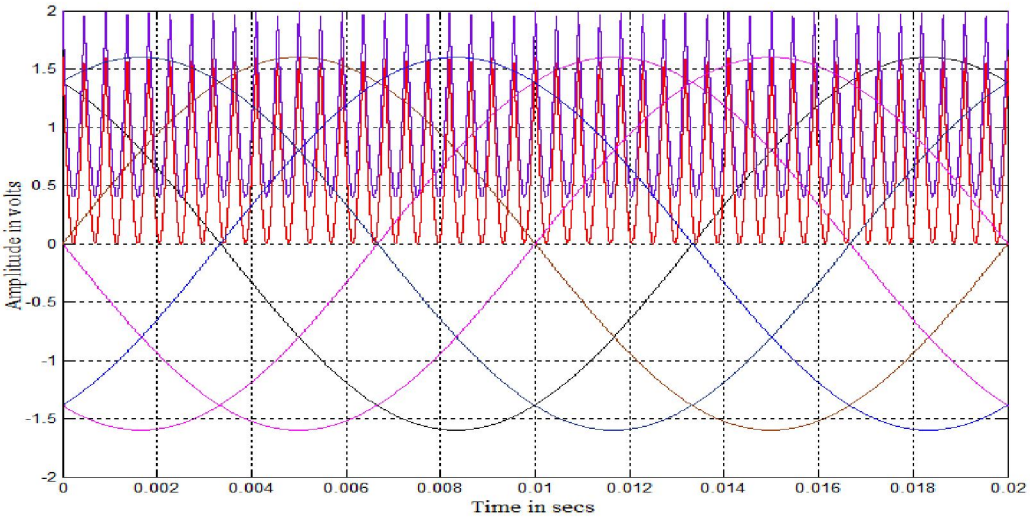

Fig. 6. Carrier Arrangements for UISCCOPWM Strategy (m_a = 0.8 , m_f = 40)

3.5 UNIPOLAR INVERTED SINE CARRIER VARIABLE FREQUENCY PWM (UISCVFPWM) STRATEGY

The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches in PDPWM using constant frequency carriers. In order to equalize the number of switching for all the switches, variable frequency PWM strategy is used as illustrated in Fig. 7

$$m_a = \frac{A_m}{(n*A_c)}$$

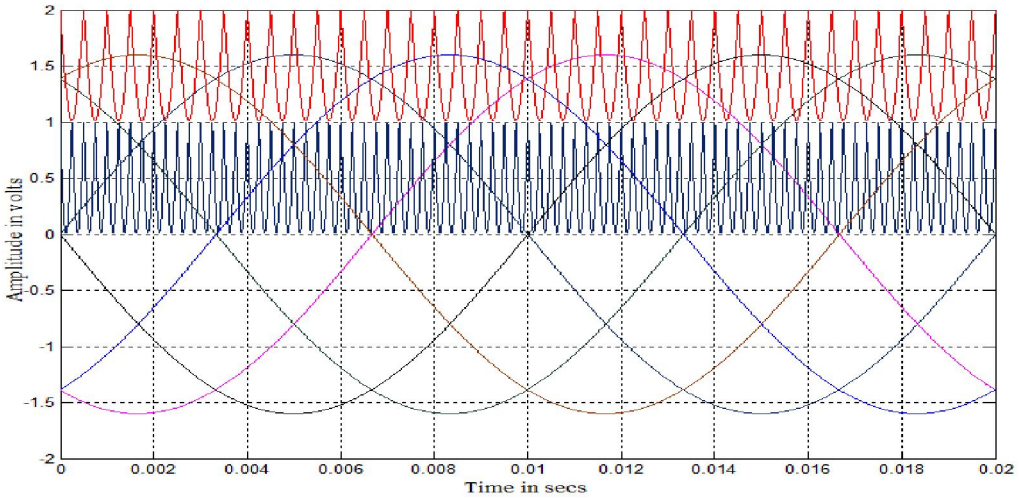

Fig. 7. Carrier Arrangements for UISCVFPWM Strategy (m_a= 0.8 , m_f = 40 for upper and lower switches and m_f = 80 for intermediate switches)

4 60 DEGREE PWM REFERENCE

This method is almost similar to sinusoidal PWM except that the modulating sine wave is flat topped for a period of 60 degree in each half cycle[11]. 60 degree PWM reference technique is as shown in Figs. 8 - 12.

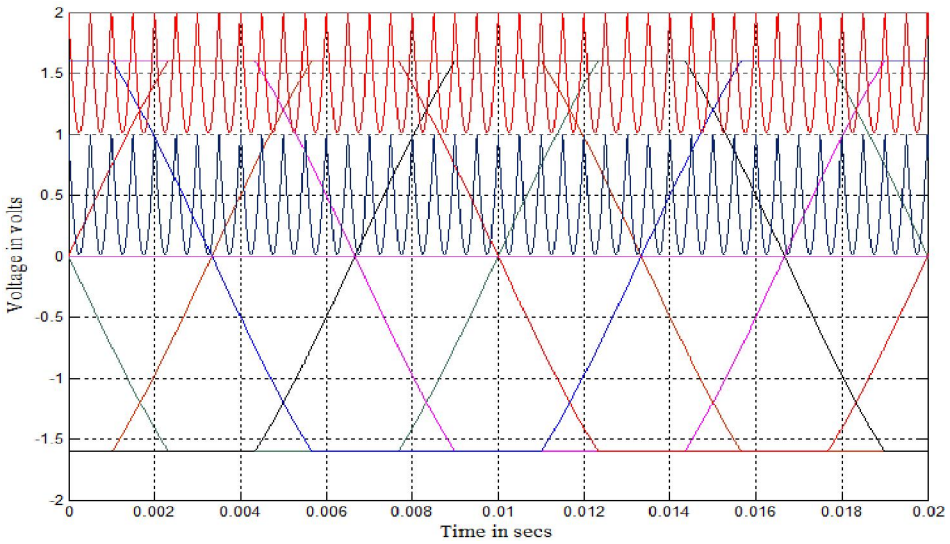

Fig. 8. Carrier Arrangements for UISCPDPWM Strategy ($m_a = 0.8$, $m_f = 40$)

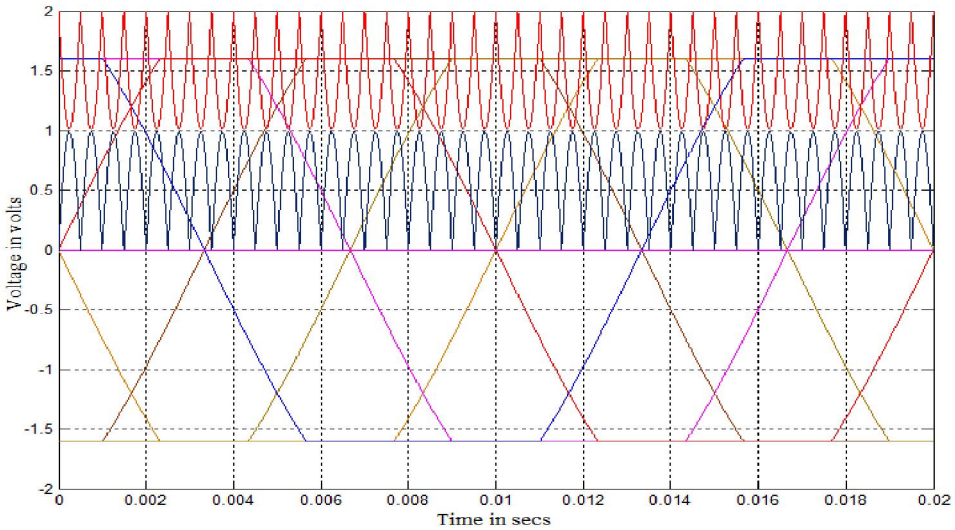

Fig. 9. Carrier Arrangements for UISCAPODPWM Strategy ($m_a = 0.8$, $m_f = 40$)

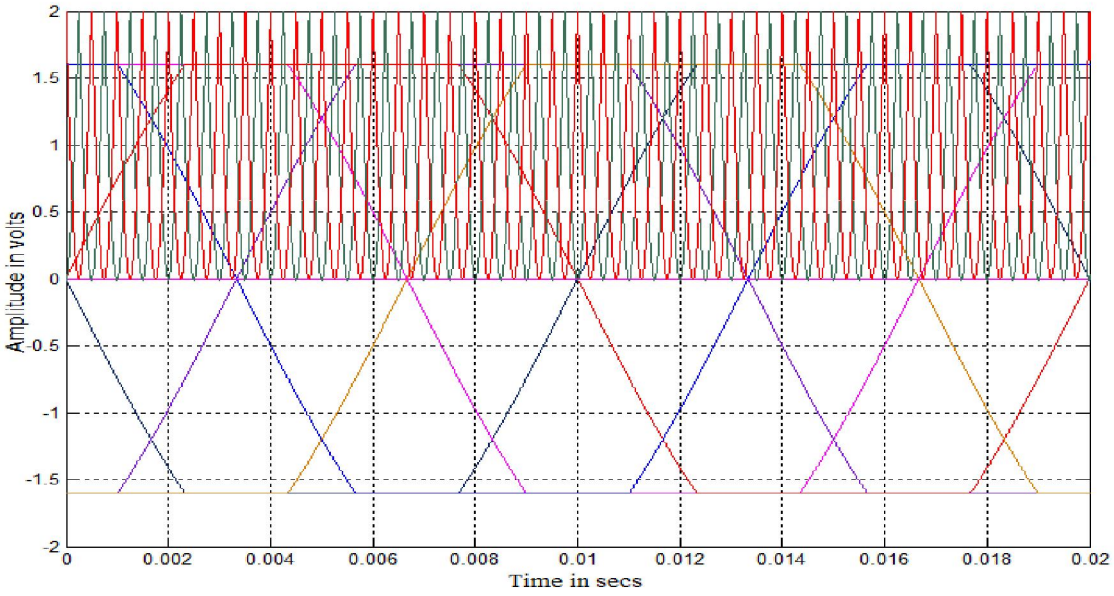

Fig. 10. Carrier Arrangements for UISCPSPWM Strategy (m_a = 0.8 , m_f = 40)

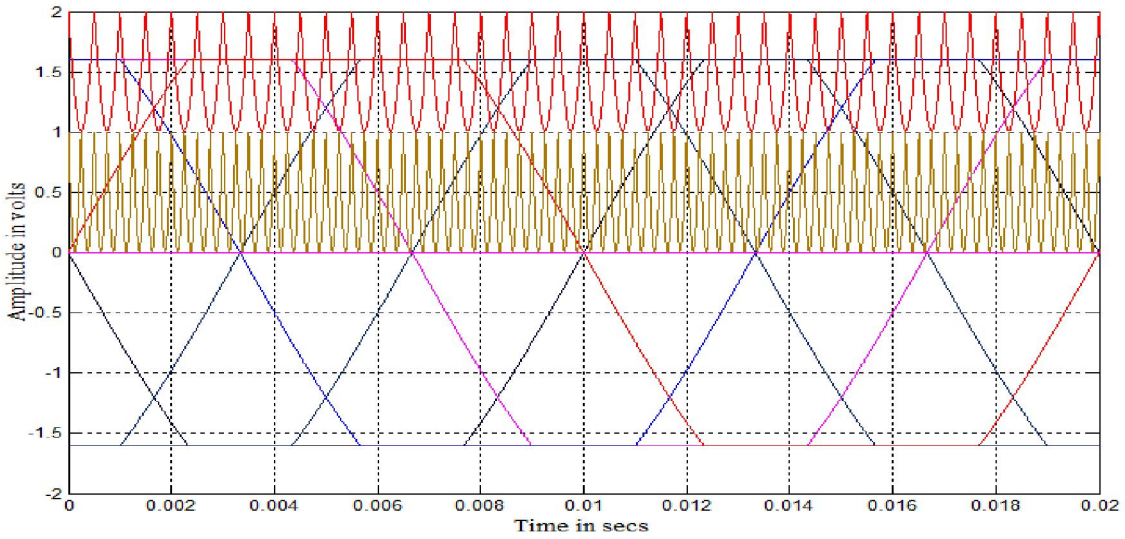

Fig. 11. Carrier Arrangements for UISCVFPWM Strategy (m_a=0.8 , m_f=40 for upper and lower switches and m_f = 80 for intermediate switches)

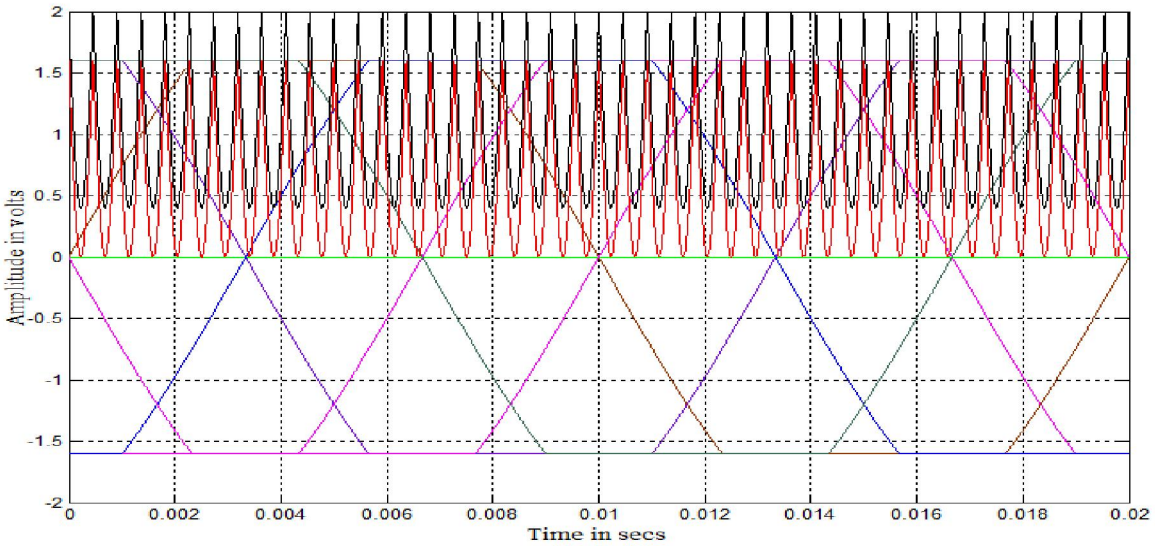

Fig. 12. Carrier Arrangements for UISCCOPWM Strategy ($m_a = 0.8$, $m_f = 40$)

5 STEPPED WAVE REFERENCE

The stepped wave is a approximation to the sine wave. It is divided into specified intervals (say 20^0) with each interval controlled individually to control magnitude of the fundamental component and to eliminate specific harmonics. This type of control gives low distortion but a higher fundamental amplitude compared with that of normal PWM control [11]. Stepped wave PWM technique is as shown in Fig. 13-17.

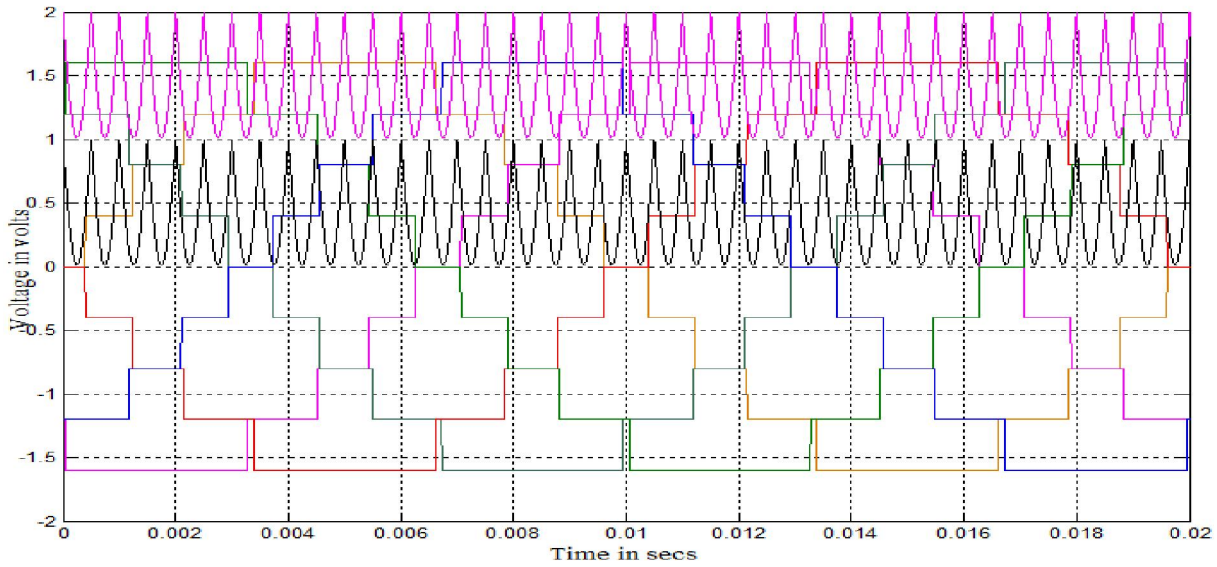

Fig. 13. Carrier Arrangements for UISCPDPWM Strategy ($m_a = 0.8$, $m_f = 40$)

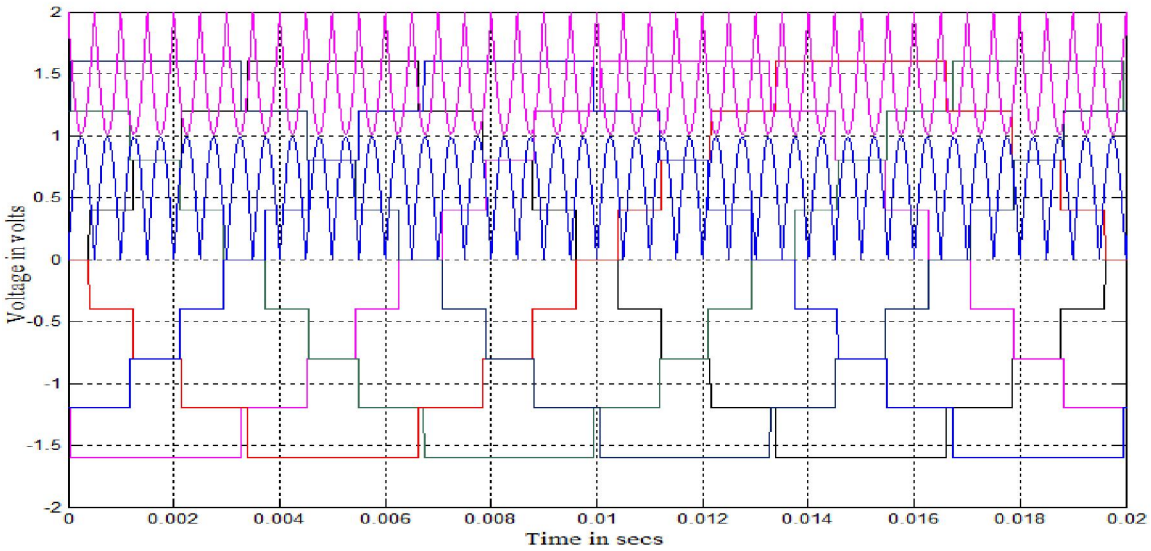

Fig. 14. Carrier Arrangements for UISCAPODPWM Strategy ($m_a = 0.8$, $m_f = 40$)

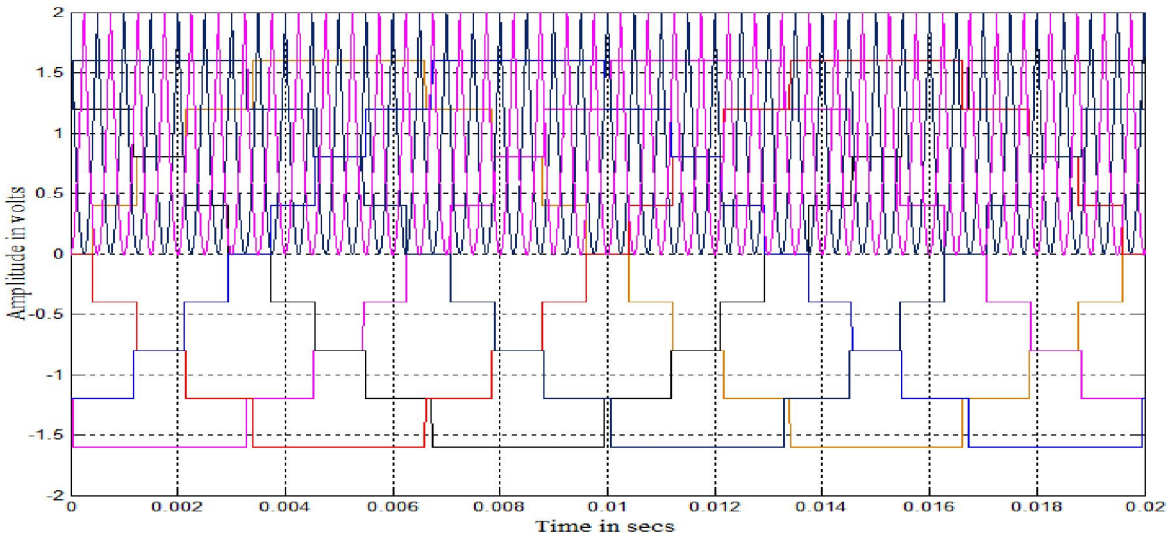

Fig. 15. Carrier Arrangements for UISCPSPWM Strategy ($m_a = 0.8$, $m_f = 40$)

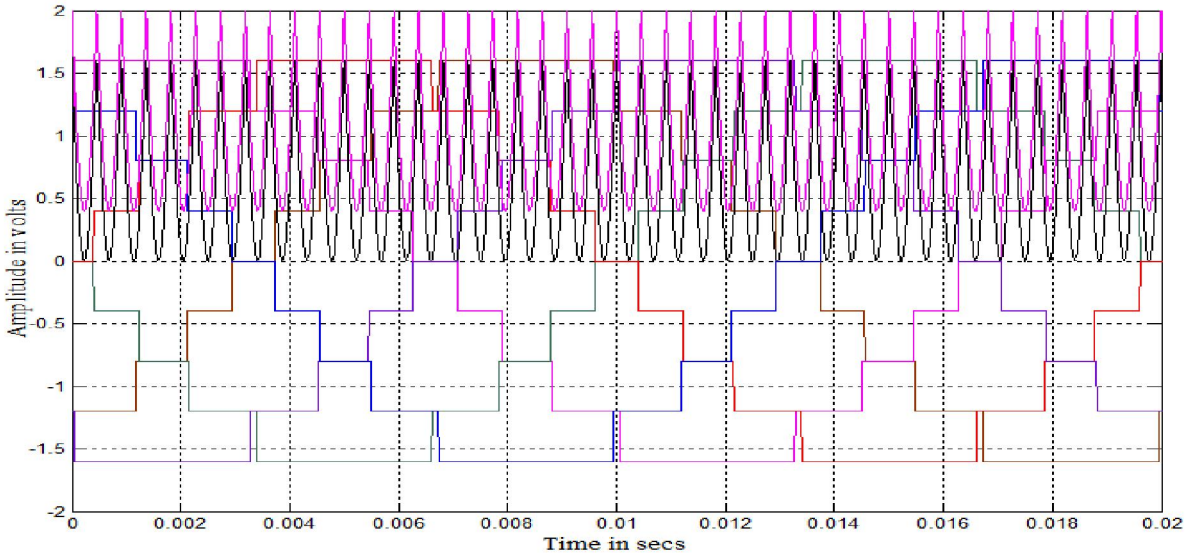

Fig. 16. Carrier Arrangements for UISCCOPWM Strategy (m_a = 0.8 , m_f = 40)

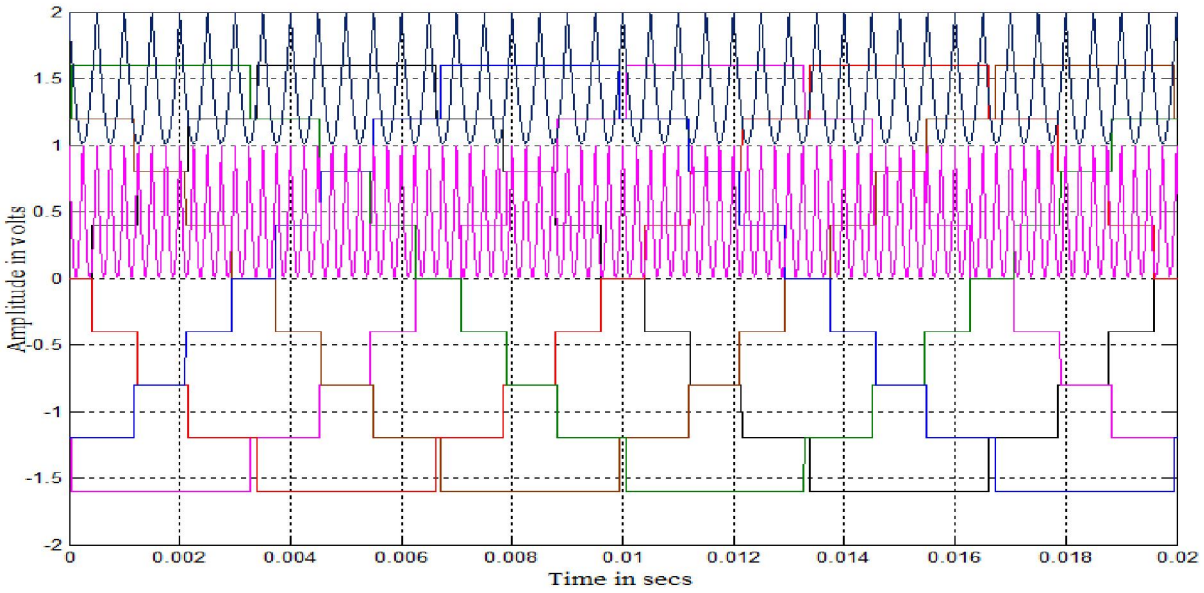

Fig. 17. Carrier Arrangements for UISCVFPWM Strategy (m_a=0.8 , m_f=40 for upper and lower switches and m_f = 80 for intermediate switches)

6 SIMULATION RESULTS

The cascaded five level inverter is modeled in SIMULINK using power system block set. Switching signals for CMLI are developed using unipolar inverted sine carrier PWM techniques discussed previously. Simulations are performed for different values of m_a ranging from 0.6 – 1. The corresponding %THD values are measured using FFT block and they are shown in Tables 1, 3 and 5. Tables 2, 4 and 6 display the V_{RMS} of fundamental of inverter output for same modulation indices. Figs. 18 - 47 show the simulated output voltages of CMLI and corresponding FFT plots for R-Phase with above strategies but for only one sample value of m_a = 0.8. Figs. 18-27 are for sine reference. Fig. 18 shows the five level output voltage generated by UISCPDPWM strategy and its FFT plot is shown in Fig. 19. From Fig. 19, it is observed that the UISCPDPWM strategy produces significant 7^{th}, 9^{th}, 31^{st}, 33^{rd} and 37^{th} harmonic energy. Fig. 20 shows the five level output voltage generated by UISCAPODPWM strategy and its FFT plot is shown in Fig. 21. From Fig. 21, it is observed that the UISCAPODPWM produces significant 3^{rd}, 5^{th}, 9^{th}, 31^{st}, 35^{th}, 37^{th} and 39^{th} harmonic energy. Fig. 22 shows the five level output voltage generated by UISCCOPWM strategy and its FFT plot is shown in Fig. 23. From Fig. 23, it is observed that the UISCCOPWM strategy produces

no significant/dominant harmonic. Fig. 24 shows the five level output voltage generated by UISCPSPWM strategy and its FFT plot is shown in Fig. 25. From Fig. 25, it is observed that the UISCPSPWM strategy produces significant 3rd, 5th and 7th harmonic energy. Fig. 26 shows the five level output voltage generated by UISCVFPWM strategy and its FFT plot is shown in Fig. 27. From Fig. 27, it is observed that the UISCVFPWM strategy produces significant 7th, 9th, 35th and 39th harmonic energy.

The next ten figures show results for 60 degree PWM strategy. Fig. 28 shows the five level output voltage generated by UISCPDPWM (60 degree) strategy and its FFT plot is shown in Fig. 29. From Fig. 29, it is observed that the UISCPDPWM (60 degree) strategy produces significant 3rd, 11th, 27th, 29th and 37th harmonic energy. Fig. 30 shows the five level output voltage generated by UISCAPODPWM (60 degree) strategy and its FFT plot is shown in Fig.31. From Fig. 31, it is observed that the UISCAPODPWM (60 degree) strategy produces significant 3rd, 5th, 7th, 27th, 31st, 33rd and 35th harmonic energy. Fig. 32 shows the five level output voltage generated by UISCCOPWM (60 degree) strategy and its FFT plot is shown in Fig. 33. From Fig. 33, it is observed that the UISCCOPWM (60 degree) strategy produces significant 3rd and 37th harmonic energy. Fig. 34 shows the five level output voltage generated by UISCPSPWM (60 degree) strategy and its FFT plot is shown in Fig. 35. From Fig. 35, it is observed that the UISCPSPWM (60 degree) strategy produces significant 3rd and 5th harmonic energy. Fig. 36 shows the five level output voltage generated by UISCVFPWM (60 degree) strategy and its FFT plot is shown in Fig. 37. From Fig. 37, it is observed that the UISCVFPWM (60 degree) strategy produces significant 3rd and 11th harmonic energy.

The next ten figures show results for stepped wave PWM strategy. Fig. 38 shows the five level output voltage generated by UISCPDPWM (stepped wave) strategy and its FFT plot is shown in Fig. 39. From Fig. 39, it is observed that the UISCPDPWM (stepped wave) strategy produces significant 15th, 21st, 23rd, 25th, 31st and 37th harmonic energy. Fig. 40 shows the five level output voltage generated by UISCAPODPWM (stepped wave) strategy and its FFT plot is shown in Fig. 41. From Fig. 41, it is observed that the UISCAPODPWM (stepped wave) strategy produces significant 3rd, 5th, 11th, 15th, 19th, 25th, 27th, 29th, 31st, 33rd, 35th and 37th harmonic energy. Fig. 42 shows the five level output voltage generated by UISCCOPWM (stepped wave) strategy and its FFT plot is shown in Fig. 43. From Fig. 43, it is observed that the UISCCOPWM (stepped wave) strategy produces significant 3rd, 7th, 9th, 21st, 23rd, 25th and 29th harmonic energy. Fig. 44 shows the five level output voltage generated by UISCPSPWM (stepped wave) strategy and its FFT plot is shown in Fig. 45. From Fig. 45, it is observed that the UISCPSPWM (stepped) strategy produces significant 3rd, 5th, 7th, 21st, 23rd and 25th harmonic energy. Fig. 46 shows the five level output voltage generated by UISCVFPWM (stepped wave) strategy and its FFT plot is shown in Fig. 47. From Fig. 47, it is observed that the UISCVFPWM (stepped wave) strategy produces significant 3rd, 11th, 15th, 23rd, 25th, 27th and 35th harmonic energy. The following parameter values are used for simulation: V_{DC} =220V and R (load) = 100 ohms.

6.1 SIMULATION RESULTS FOR SINUSOIDAL REFERENCE

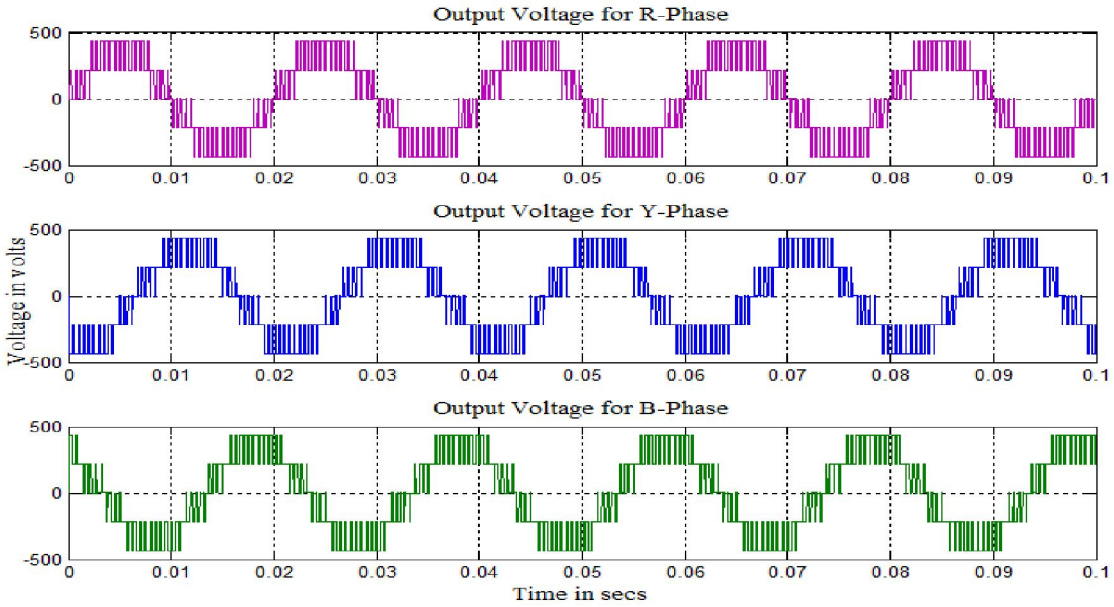

Fig. 18. Output Voltage Generated by UISCPDPWM Strategy

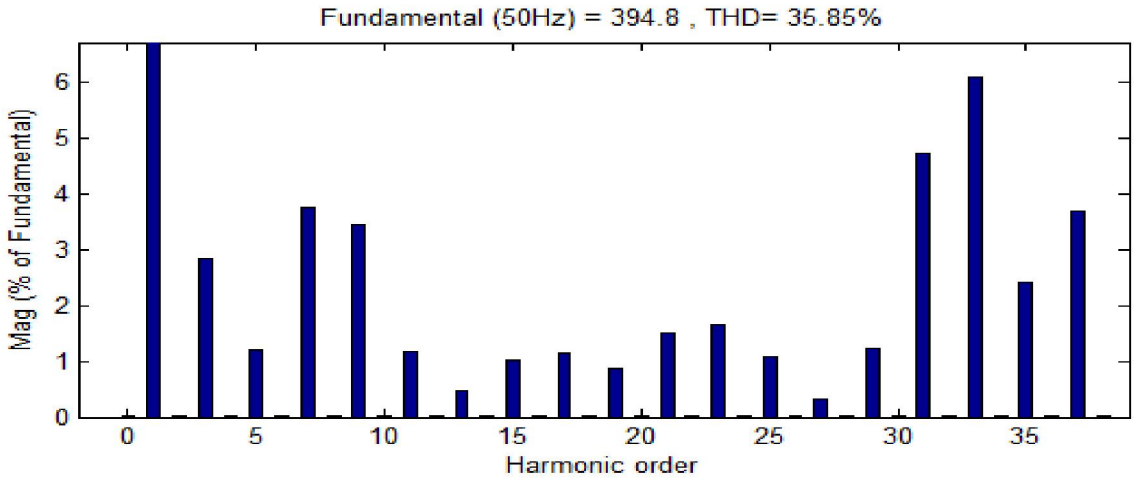

Fig. 19. FFT Plot for Output Voltage of UISCPDPWM Strategy

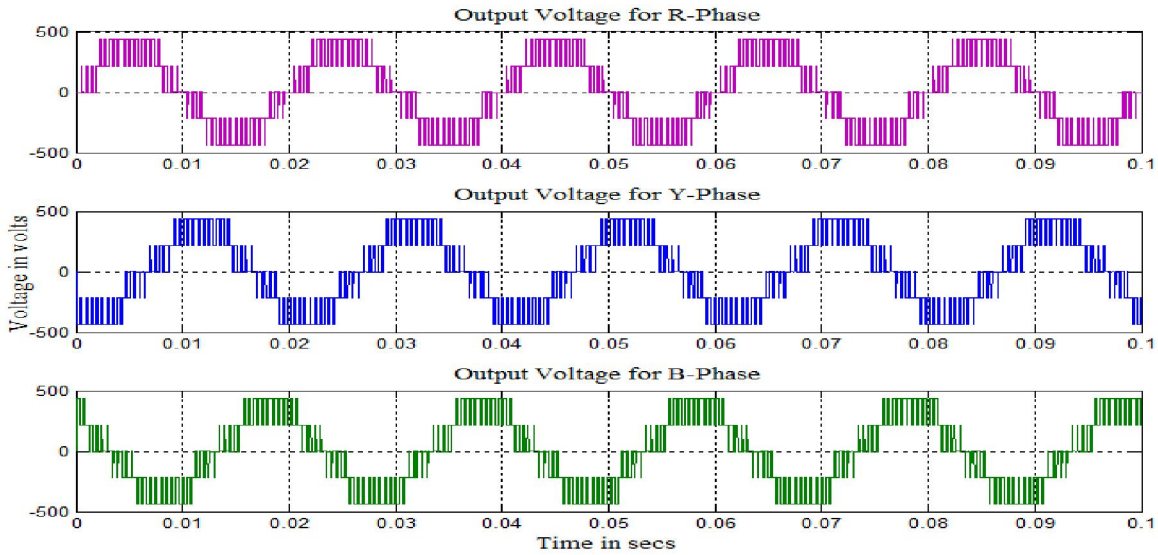

Fig. 20. Output Voltage Generated by UISCAPODPWM Strategy

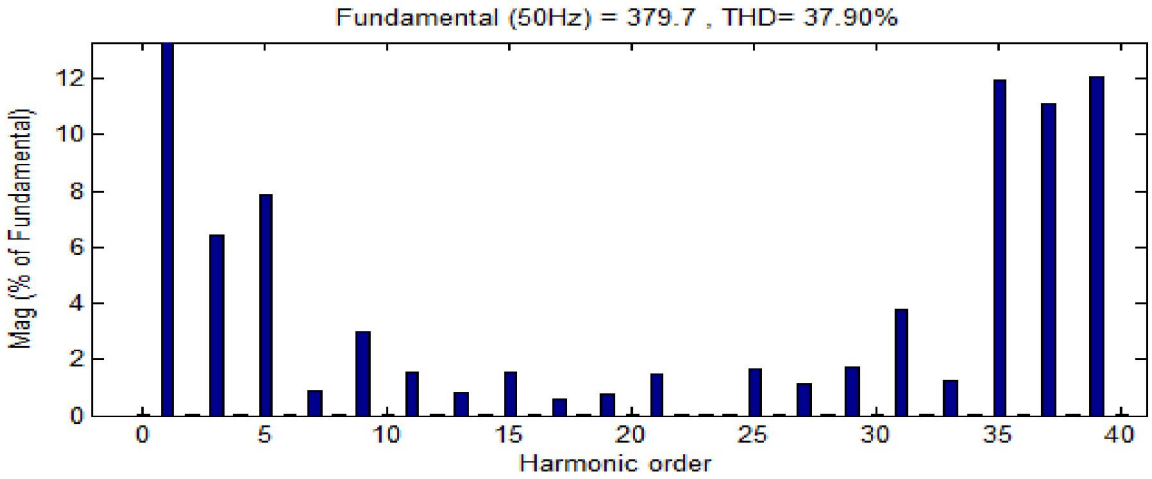

Fig. 21. FFT Plot for Output Voltage of UISCAPODPWM Strategy

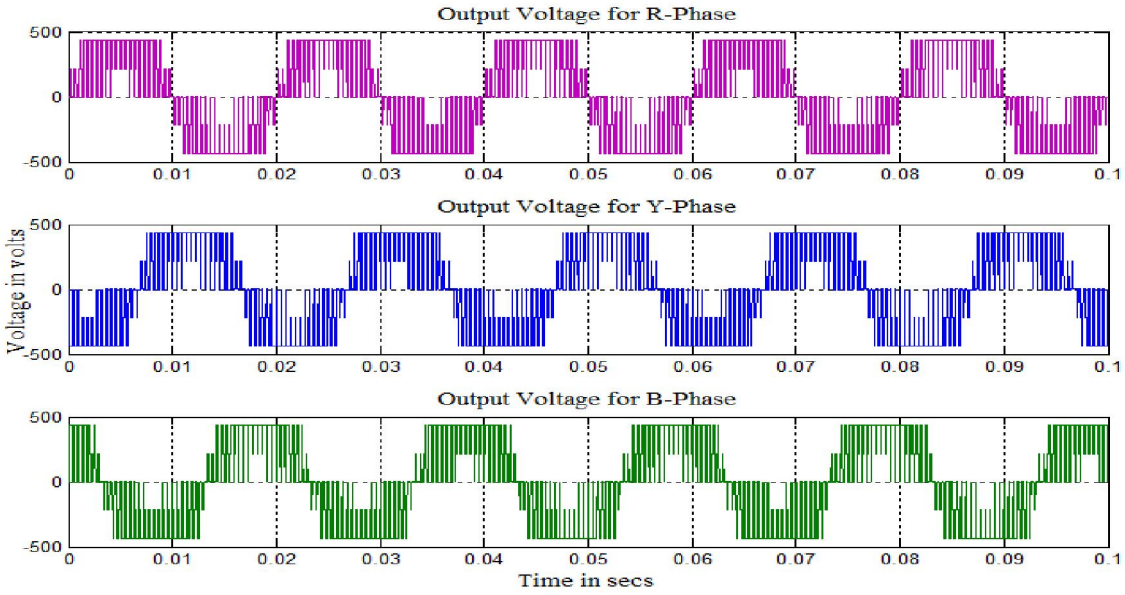

Fig. 22. Output Voltage Generated by UISCCOPWM Strategy

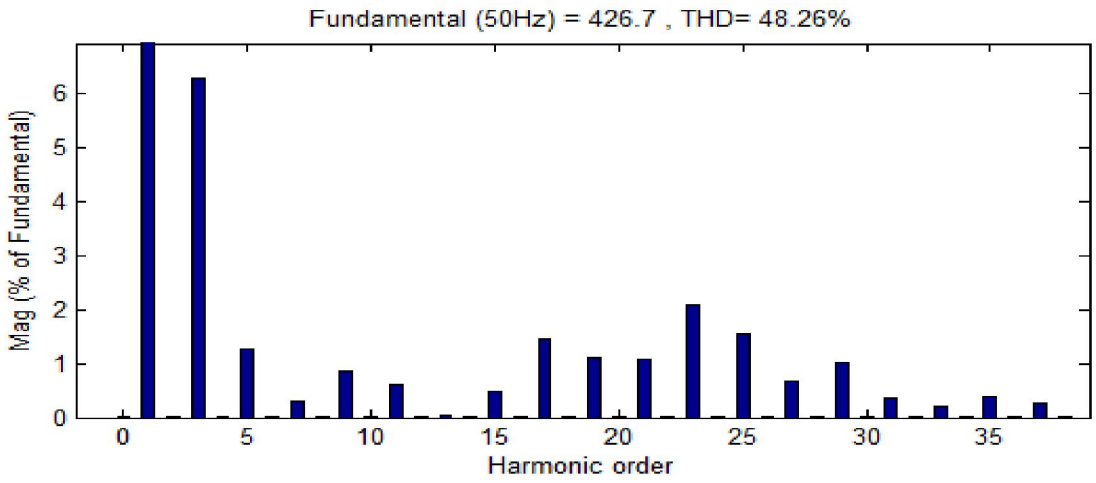

Fig. 23. FFT Plot for Output Voltage of UISCCOPWM Strategy

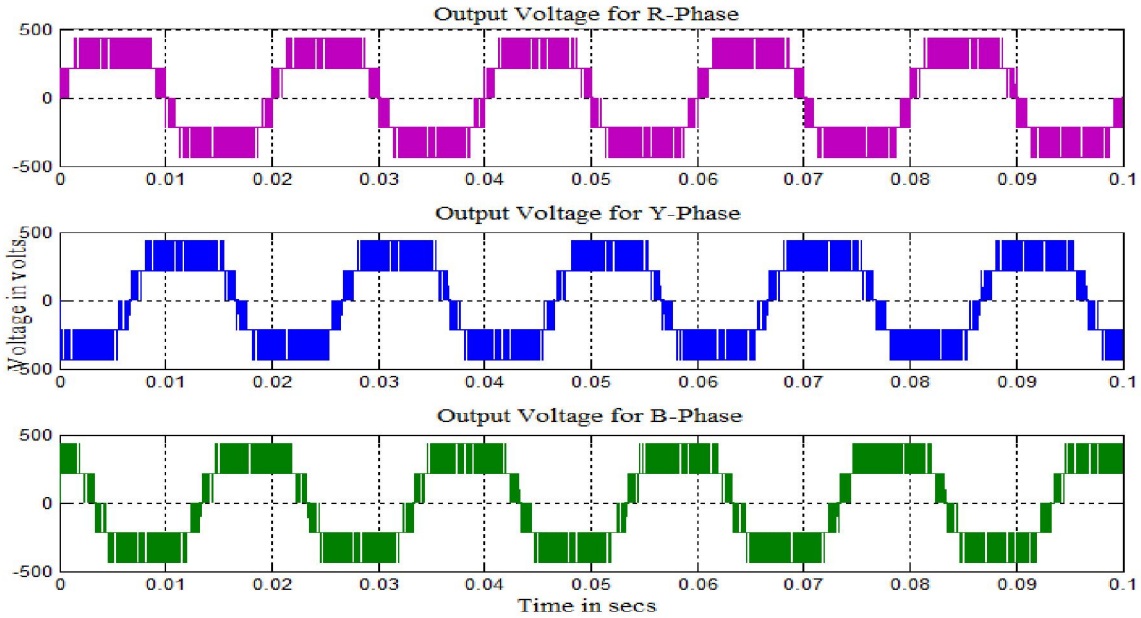

Fig. 24. Output Voltage Generated by UISCPSPWM Strategy

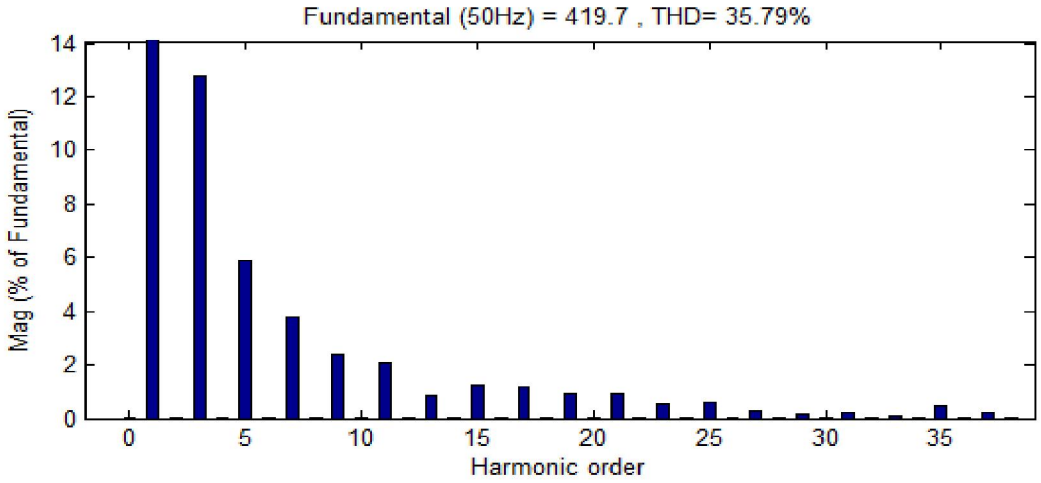

Fig. 25. FFT Plot for Output Voltage of UISCPSPWM Strategy

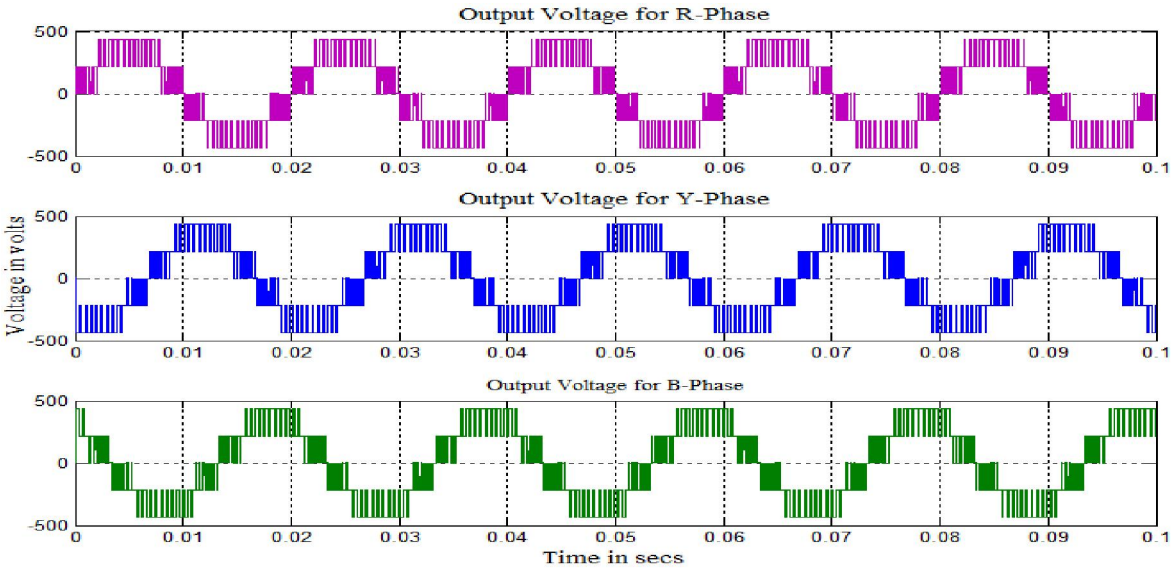

Fig. 26. Output Voltage Generated by UISCVFPWM Strategy

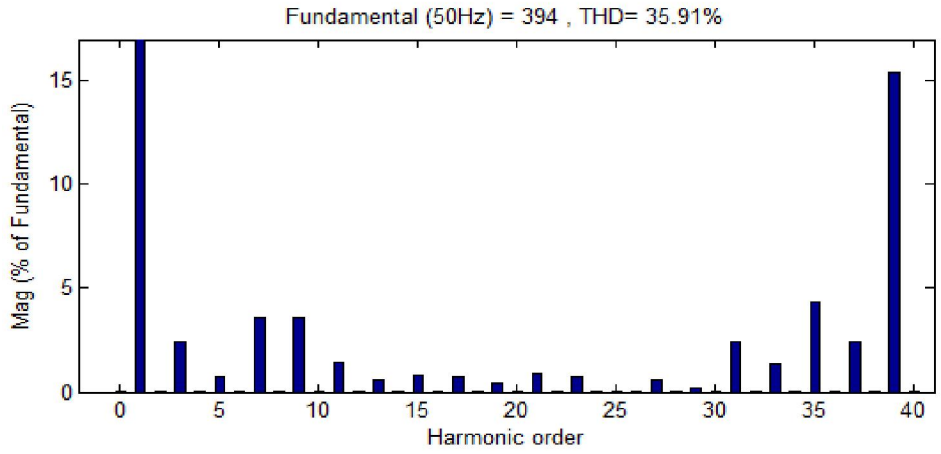

Fig. 27. FFT Plot for Output Voltage of UISCVFPWM Strategy

6.2 SIMULATION RESULTS FOR 60 DEGREE PWM REFERENCE

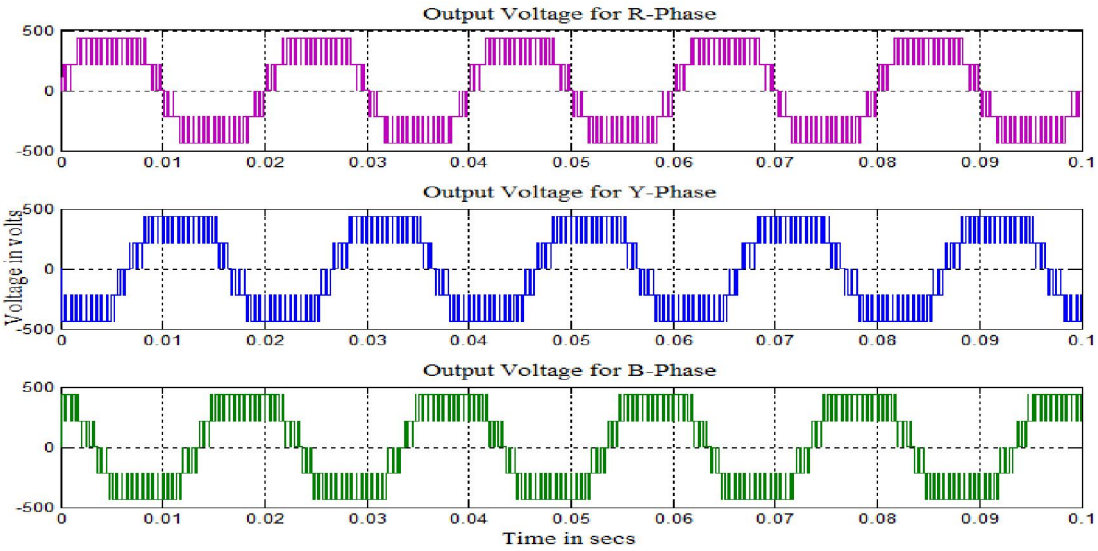

Fig. 28. Output Voltage Generated by UISCPDPWM Strategy

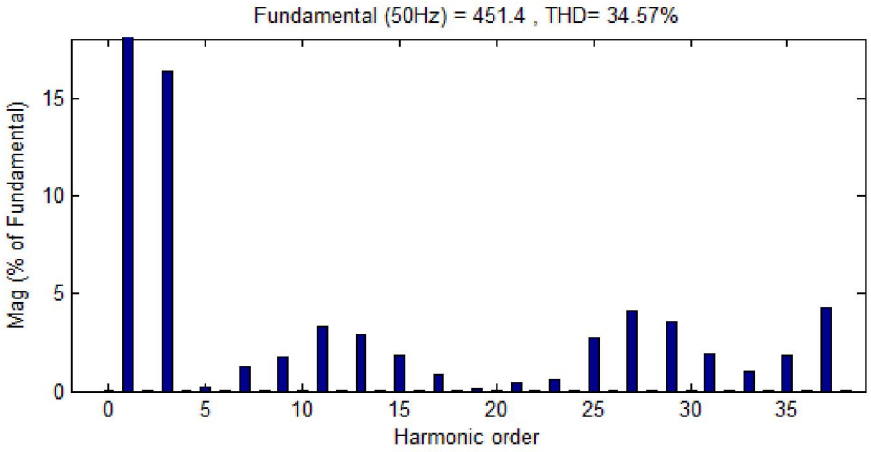

Fig. 29. FFT Plot for Output Voltage of UISCPDPWM Strategy

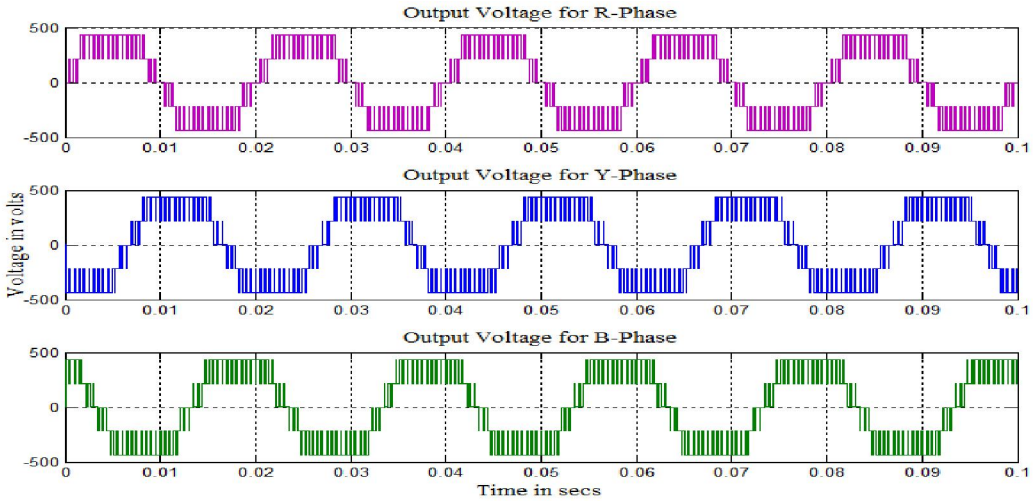

Fig. 30. Output Voltage Generated by UISCAPODPWM Strategy

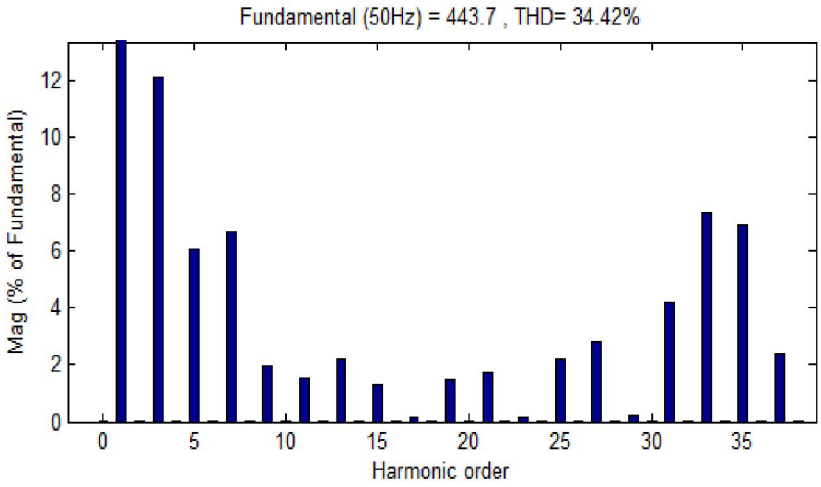

Fig. 31. FFT Plot for Output Voltage of UISCAPODPWM Strategy

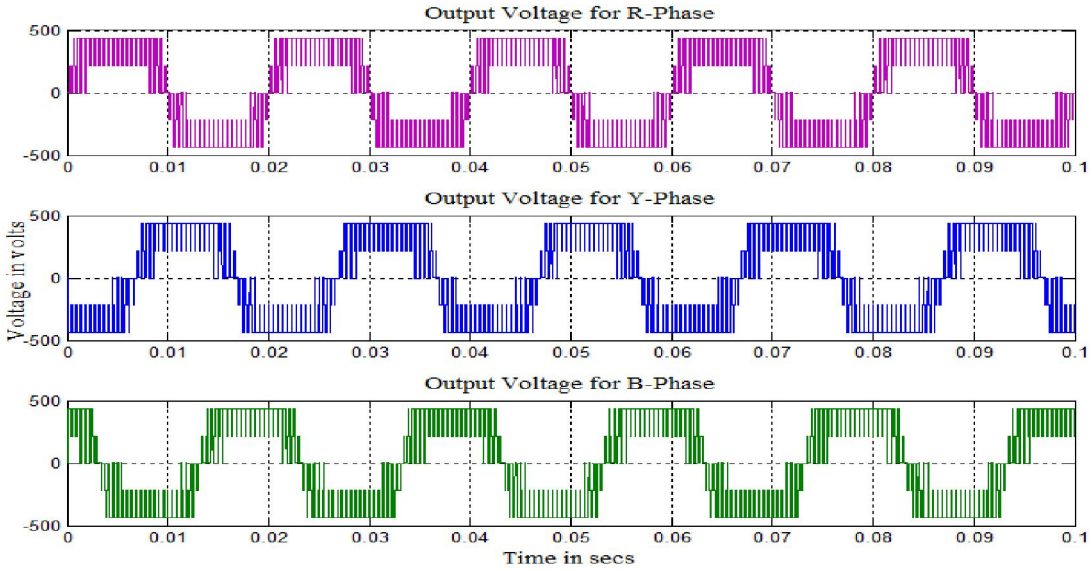

Fig. 32. Output Voltage Generated by UISCCOPWM Strategy

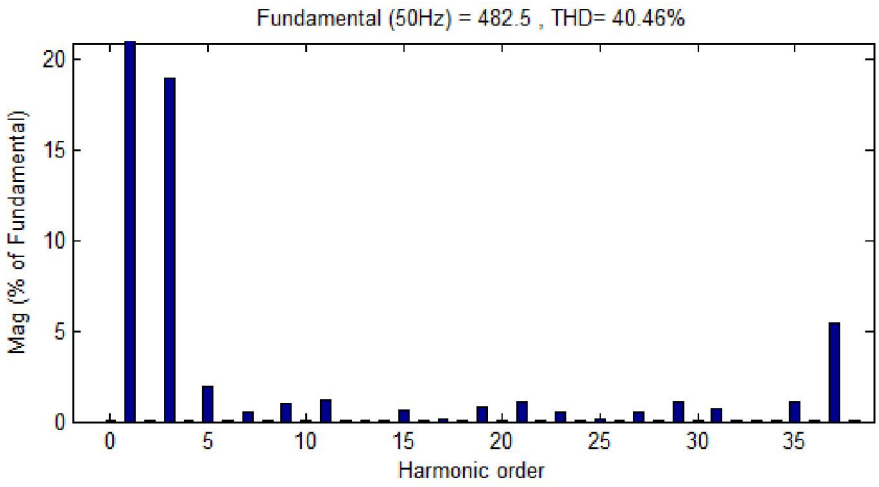

Fig. 33. FFT Plot for Output Voltage of UISCCOPWM Strategy

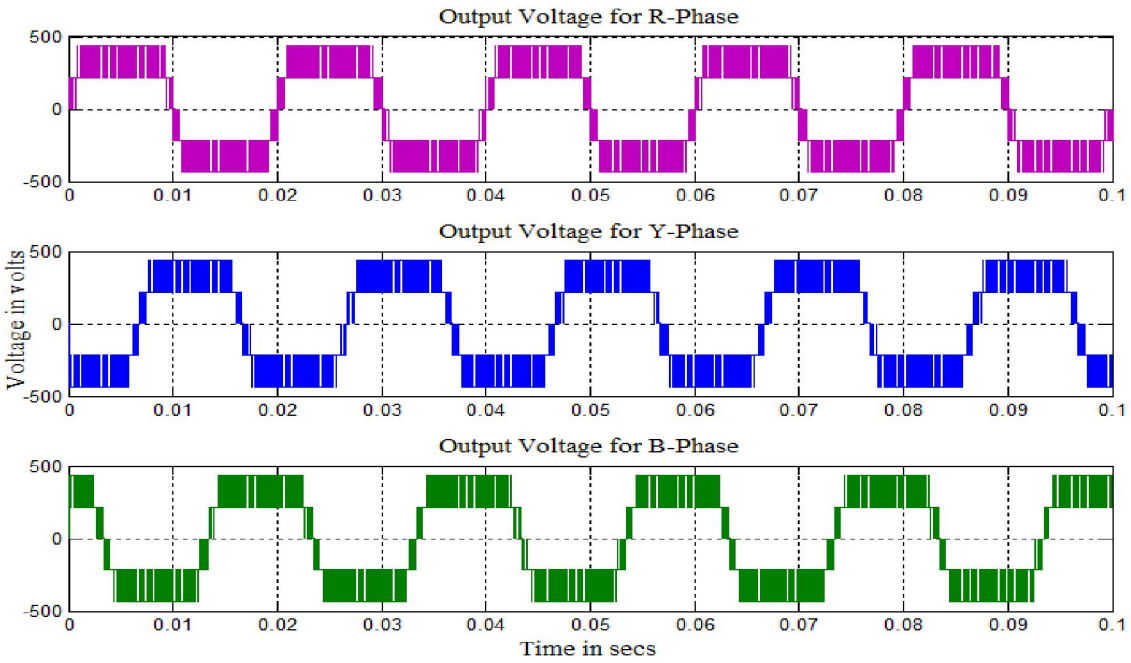

Fig. 34. Output Voltage Generated by UISCPSPWM Strategy

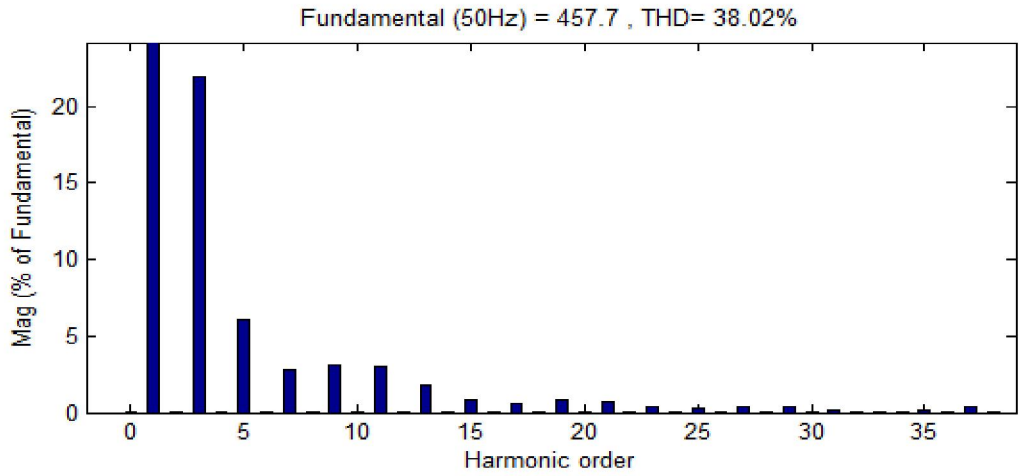

Fig. 35. FFT Plot for Output Voltage of UISCPSPWM Strategy

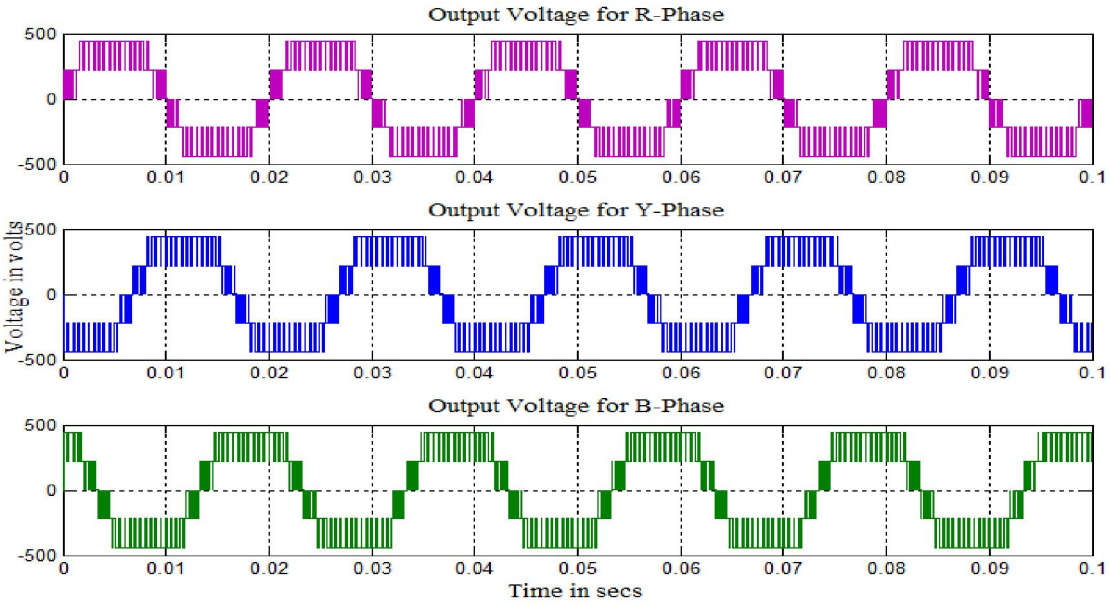

Fig. 36. Output Voltage Generated by UISCVFPWM Strategy

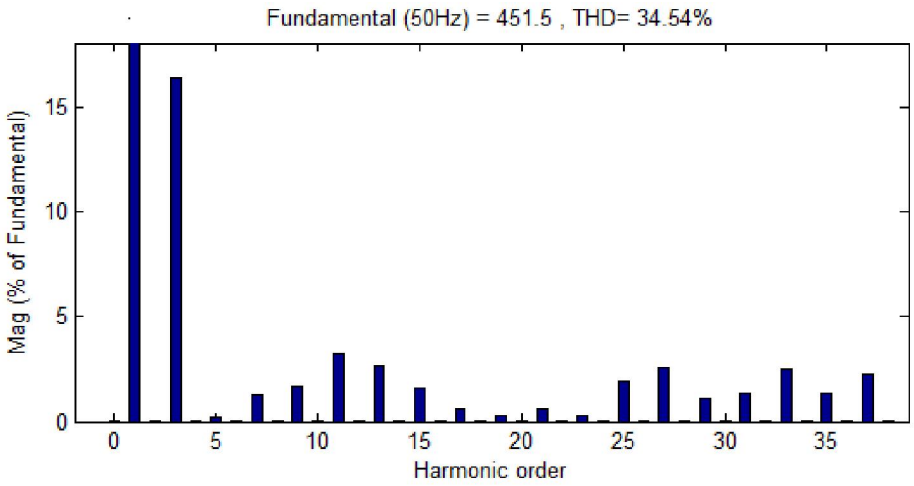

Fig. 37. FFT Plot for Output Voltage of UISCVFPWM Strategy

6.3 SIMULATION RESULTS FOR STEPPED WAVE PWM TECHNIQUE

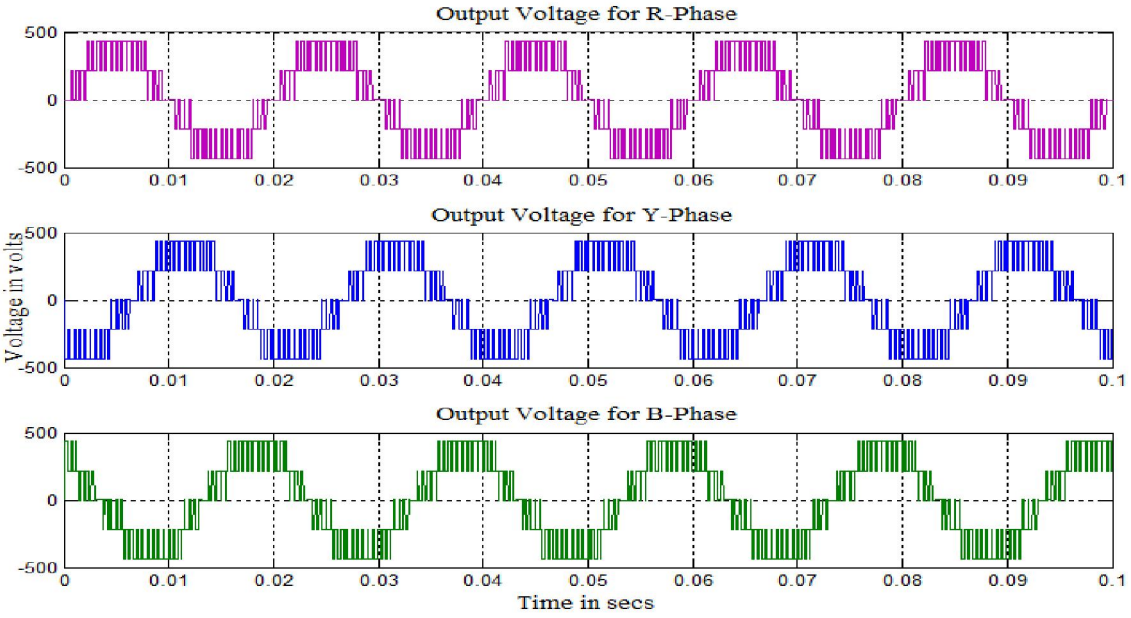

Fig. 38. Output Voltage Generated by UISCPDPWM Strategy

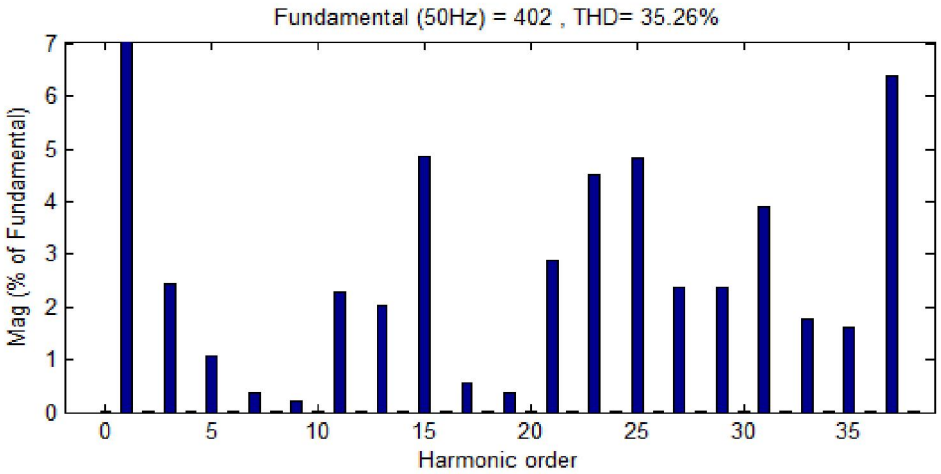

Fig. 39. FFT Plot for Output Voltage of UISCPDPWM Strategy

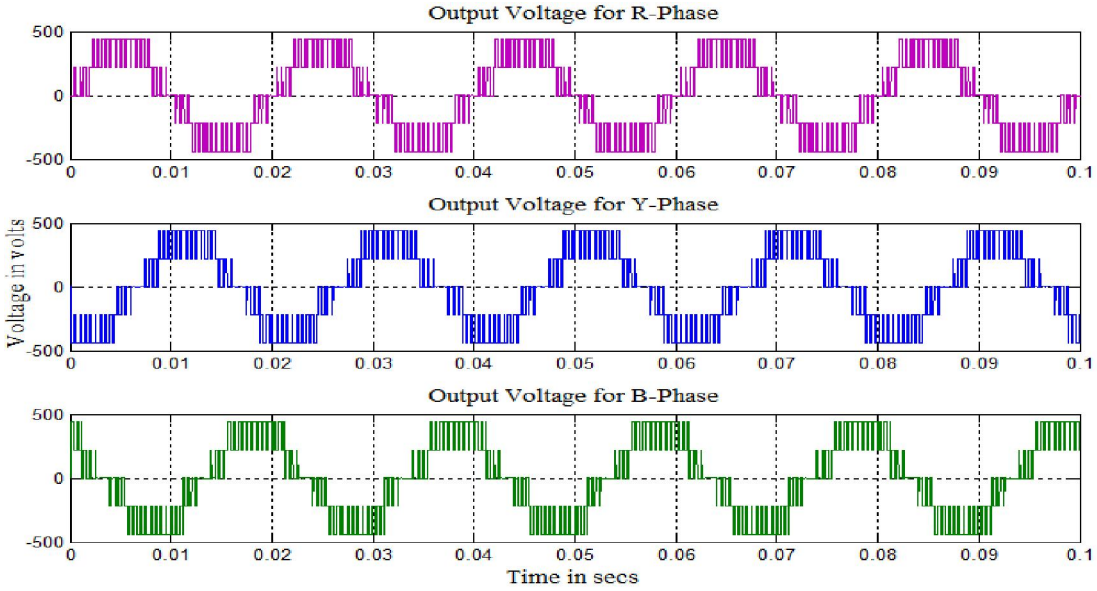

Fig. 40. Output Voltage Generated by UISCAPODPWM Strategy

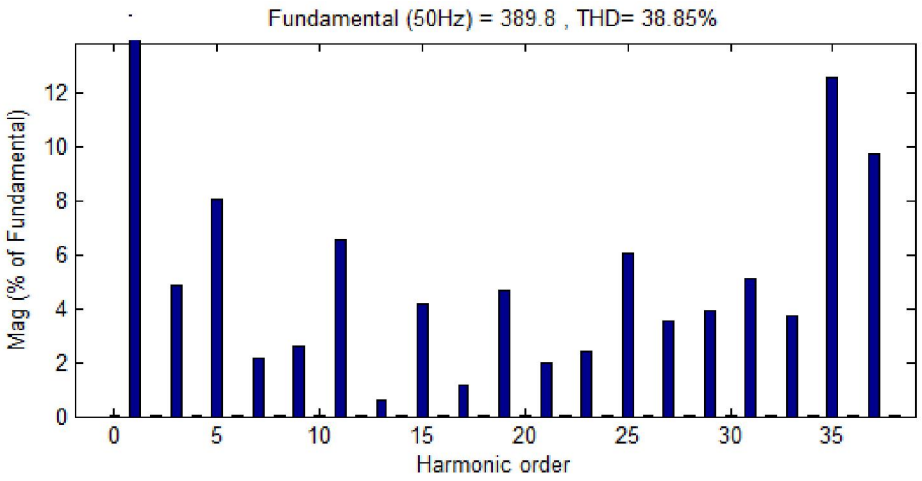

Fig. 41. FFT Plot for Output Voltage of UISCAPODPWM Strategy

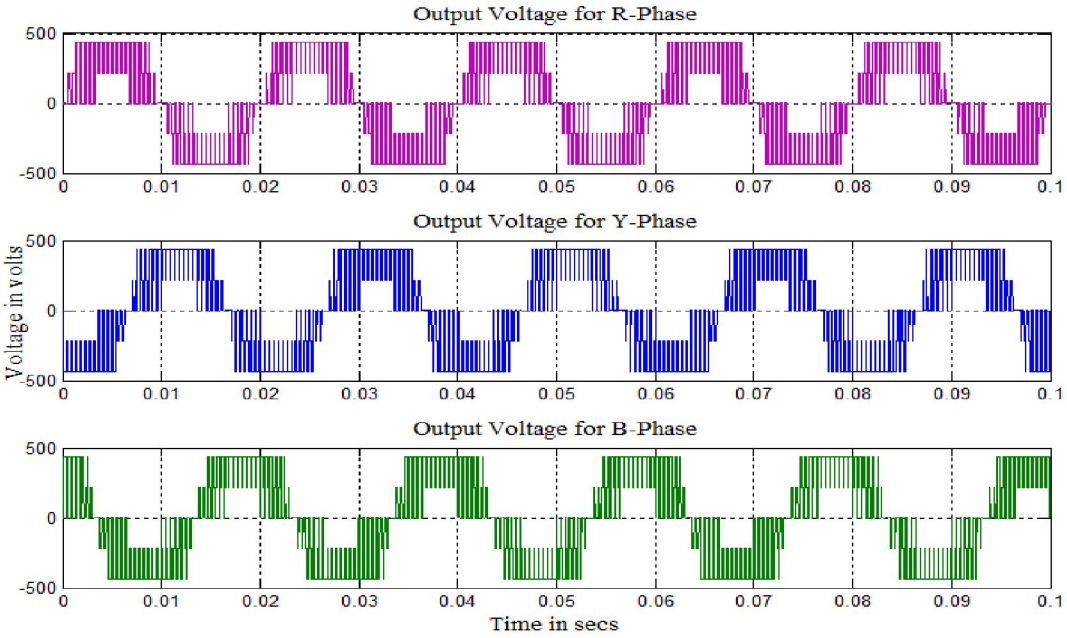

Fig. 42. Output Voltage Generated by UISCCOPWM Strategy

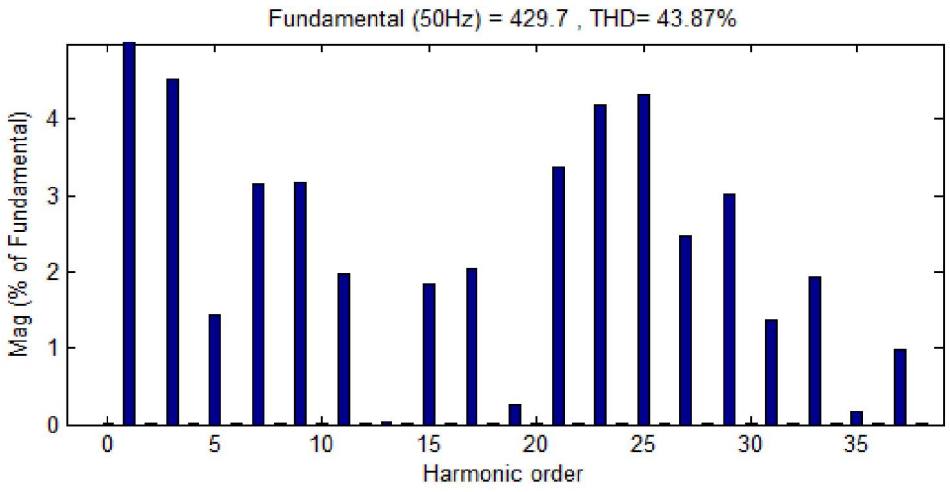

Fig. 43. FFT Plot for Output Voltage of UISCCOPWM Strategy

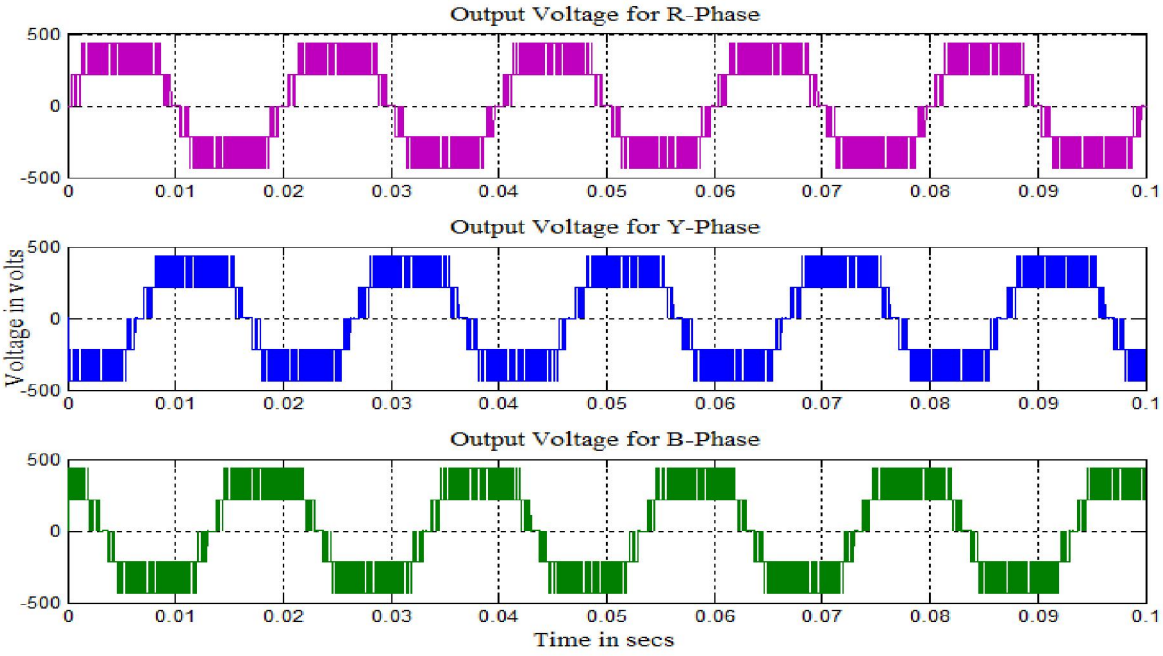

Fig. 44. Output Voltage Generated by UISCPSPWM Strategy

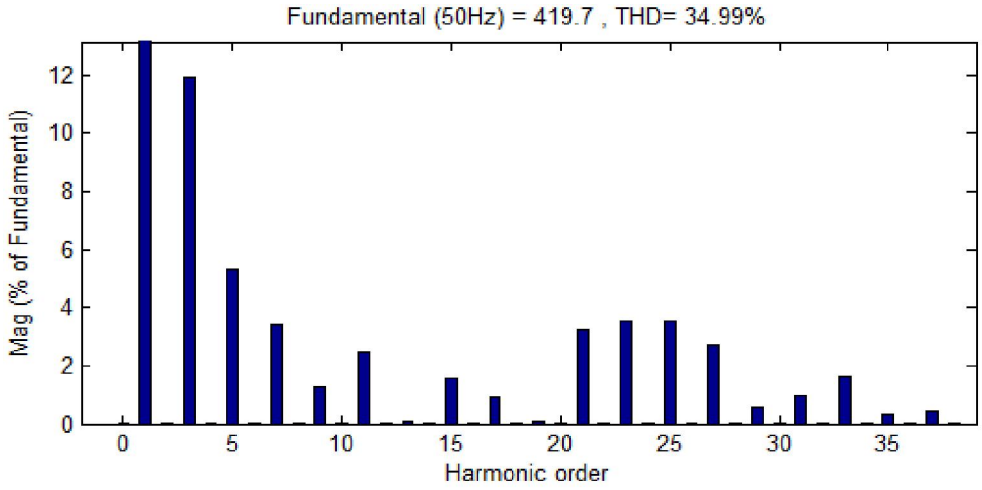

Fig. 45. FFT Plot for Output Voltage of UISCPSPWM Strategy

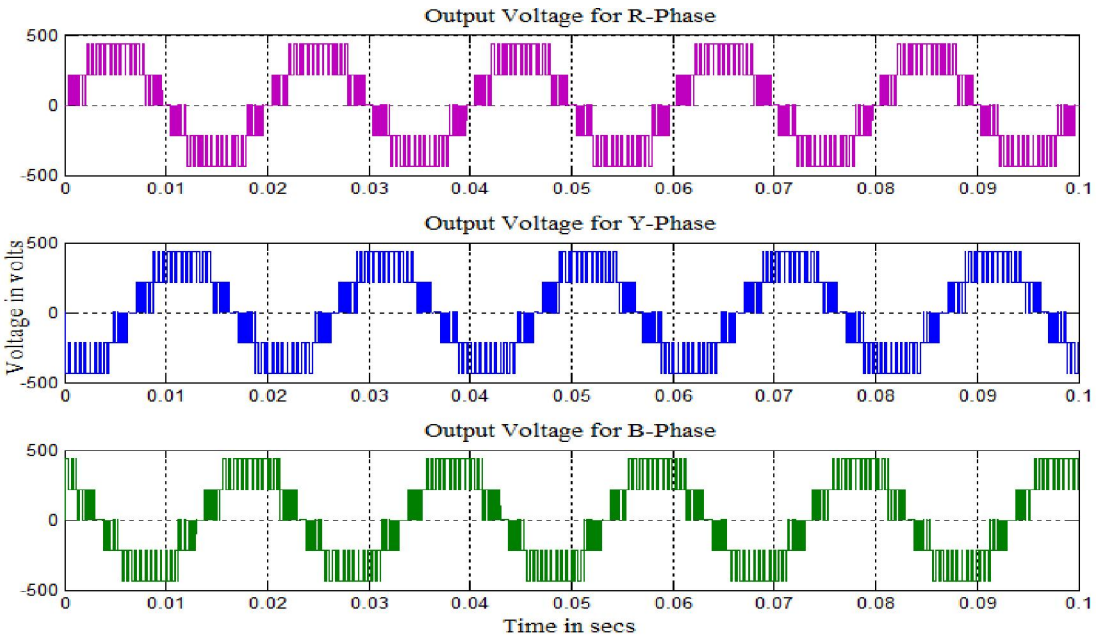

Fig. 46. Output Voltage Generated by UISCVFPWM Strategy

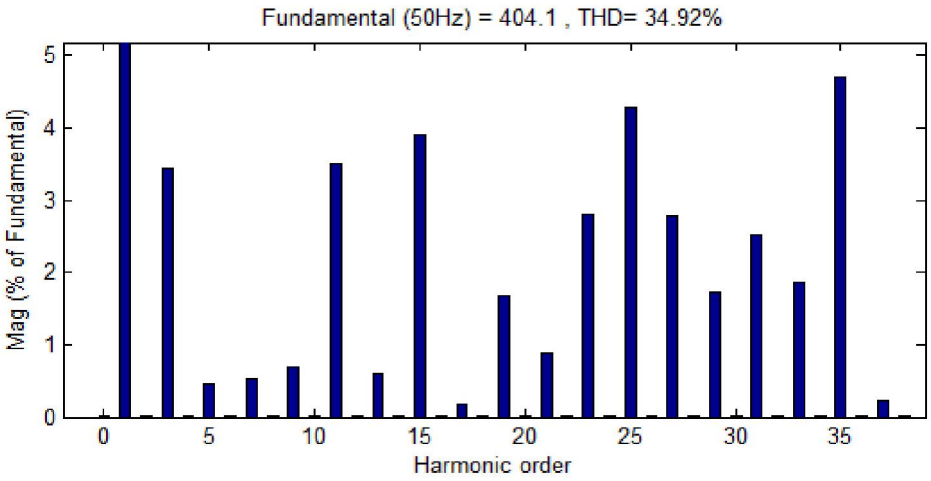

Fig. 47. FFT Plot for Output Voltage of UISCVFPWM Strategy

Table 1. % THD for Different Modulation Indices with Sinusoidal Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	26.74	26.85	37.20	28.76	26.46
0.9	30.97	32.84	40.89	32.05	30.87
0.8	35.85	37.90	48.26	35.79	35.91
0.7	40.08	44.53	58.12	38.43	40.27
0.6	44.87	52.58	68.97	40.45	44.38

Table 2. V_{RMS} (fundamental) for Different Modulation Indices with Sinusoidal Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	328.7	322.5	342.2	338.1	328.9
0.9	304.7	295.7	325.2	318.5	304.8
0.8	279.1	268.5	301.7	296.8	278.6
0.7	249.8	234.6	275	275.1	249.5
0.6	213.6	191.7	244.3	253.7	214

Table 3. % THD for Different Modulation Indices with 60 Degree PWM Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	25.74	24.64	33.16	28.73	25.57
0.9	31.19	29.91	36.95	32.57	31.00
0.8	34.57	34.42	40.46	38.02	34.54
0.7	39.54	39.44	51.11	39.46	39.64
0.6	42.20	43.11	61.57	43.07	42.13

Table 4. V_{RMS} (fundamental) for Different Modulation Indices with 60 Degree PWM Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	370.6	367.7	375.3	371.6	370.6
0.9	343.2	340.8	359	352.1	343.4
0.8	319.2	313.7	341.2	323.6	319.2
0.7	289.7	283.5	311.7	306.7	289.4
0.6	257.2	248.1	278.1	277.8	257.3

Table 5. % THD for Different Modulation Indices with Stepped Wave Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	21.79	23.23	36.18	26.88	22.01
0.9	29.33	32.90	40.76	30.50	29.02
0.8	35.26	38.85	43.87	34.99	34.92
0.7	39.30	43.02	54.42	36.36	39.65
0.6	42.60	56.73	65.61	38.21	42.32

Table 6. V_{RMS} (fundamental) for Different Modulation Indices with Stepped Wave Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	330.3	327.2	344.7	336.6	330.9
0.9	307.1	299.5	325.6	319.2	309
0.8	284.2	275.6	303.9	296.8	285.7
0.7	249	239	275.9	280.7	249.9
0.6	216	190.5	245.9	252.1	217.2

Table 7. Crest Factor (CF) for Different Modulation Indices with Sinusoidal Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	1.4140	1.4142	1.4140	1.4140	1.4144
0.9	1.4145	1.4139	1.4142	1.414	1.4143
0.8	1.4145	1.4141	1.4143	1.4140	1.4142
0.7	1.4143	1.4143	1.4138	1.4143	1.4144
0.6	1.4143	1.4141	1.4142	1.4138	1.4144

Table 8. Crest Factor (CF) for Different Modulation Indices with 60 Degree PWM Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	1.4141	1.4141	1.4140	1.4141	1.4144
0.9	1.4143	1.4143	1.4142	1.4140	1.4140
0.8	1.4141	1.4144	1.4141	1.4144	1.4144
0.7	1.4142	1.4141	1.4141	1.4144	1.4143
0.6	1.4144	1.4143	1.4142	1.4143	1.4143

Table 9. Crest Factor (CF) for Different Modulation Indices with Stepped Wave Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	1.4144	1.4144	1.4139	1.4144	1.4143
0.9	1.4141	1.4143	1.4143	1.4141	1.4142
0.8	1.4144	1.4136	1.4139	1.4140	1.4144
0.7	1.4140	1.4142	1.4139	1.4139	1.4141
0.6	1.4143	1.4141	1.4143	1.4141	1.4139

Table 10. Form factor for Different Modulation Indices with Sinusoidal Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	INF	INF	INF	INF	INF
0.9	INF	INF	INF	INF	INF
0.8	INF	INF	INF	INF	INF
0.7	INF	INF	INF	INF	INF
0.6	INF	INF	INF	INF	INF

Table 11. Form factor for Different Modulation Indices with 60 Degree PWM Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	INF	INF	INF	INF	INF
0.9	INF	INF	INF	INF	INF
0.8	INF	INF	INF	INF	INF
0.7	INF	INF	INF	INF	INF
0.6	INF	INF	INF	INF	INF

Table 12. Form factor for Different Modulation Indices with Stepped Wave Reference

m_a	UISCPD	UISCAPOD	UISCCO	UISCPS	UISCVF
1	INF	INF	INF	INF	INF
0.9	INF	INF	INF	INF	INF
0.8	INF	INF	INF	INF	INF
0.7	INF	INF	INF	INF	INF
0.6	INF	INF	INF	INF	INF

7 CONCLUSION

It is observed from Tables 1, 3 and 5 that UISCAPODPWM with 60 degree PWM reference provides output with relatively low distortion, UISCPSPWM and UISCVFPWM with sine and stepped wave references respectively also provide output with relatively low distortion. For all three chosen references UISCCOPWM is found to perform better since it provides relatively higher fundamental RMS output voltage (Tables 2, 4 and 6) and UISCCOPWM with 60 degree PWM is found to provide highest output. Tables 7, 8 and 9 provide crest factor and Tables 10, 11 and 12 provide FF for all modulating indices. Depending on the performance measure required in a particular application of chosen MLI based on the expected output quality, appropriate PWM may be employed.

REFERENCES

[1] Fang Zhang Peng, "A generalized multilevel inverter topology with self voltage balancing, " *IEEE Trans. on Industry Applications*, vol. 37, n°. 2, pp. 611- 618, 2001.

[2] Jose Rodriguez, Jih-Sheng Lai, and Fang Zheng, "Multilevel Inverters: A Survey of Topologies, Controls and Applications," *IEEE Transactions on Power Electronics*, vol. 49, n°. 4, pp.724-738, 2002.

[3] C. Keith, A. Wielebski Mike, W. Peng Fang, and J. Wang, "Control of cascaded multilevel inverter," *IEEE Transaction on Power Electronics,* vol. 19, n°. 3, pp.732-738, 2004.

[4] S. Jeevananthan, R. Nandhakumar, and P. Dananjayan, "Inverted sine carrier for fundamental fortification in PWM inverters and fpga based implementations," *Serbian Journal of Electrical Engineering*, vol. 4, n°. 2, pp. 171-187, 2007.

[5] R. Gupta, A. Ghosh, and A. Joshi, "Switching characteristics of cascaded multilevel controlled systems," *IEEE Trans. on Industrial Electronics,* vol. 55, n°. 3, pp. 1047-1057, 2008.

[6] M. Malinowski, K. Gopakumar, J. Rodriguez, and A. Perez, "A Survey on Cascaded Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, n°.7, pp 2197-2206, July 2010.

[7] R. Seyezhai, and B.L. Mathur, "Hybrid multilevel inverter using ISPWM technique for single phase inverter," *International Journal of Computer Applications,* vol. 2, pp. 602-610, 2012.

[8] A. Maiti, "Development of microcontroller based ISPWM Switching technique for single phase inverter," *International Journal of Engineering Science and Technology,* vol. 3, n°. 6, pp.5298-5305, 2011.

[9] R. Seyezhai, and B.L. Mathur, "Inverted sine pulse width modulated three phase cascaded multilevel inverter," *International Journal of Advances in Engineering and Technology,* vol. 2, pp. 602-610, 2010.

[10] R. Bensraj, S.P. Natarajan, and B. Shanthi, "Unipolar pwm using trapezoidal amalgamated rectangular function for improved performance of multilevel inverter," *International Journal of Computer Applications,* vol. 7, n°. 13, pp 19 – 24, 2010.

[11] B. Urmila, D. Subbarayudu, "Multilevel Inverters : A comparative study of pulse width modulation techniques, " *Journal of scientific and engineering research*, vol. 1, n°. 13, pp. 1-5, 2010.